深圳市勋瑞光电科技有限公司
Xunrui photoelectric technology （shenzhen） CO,.LTD.

Product Specification

Customer: _____

Model Name: H040BWV40I3506-CT2

Date: A0

Version: 2023.04.24

■ **Preliminary Specification**

☐ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
A0	2023.04.24	Preliminary release	

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：3SPI-RGB 18bits
3) Driver IC：NV3052C TP IC: GT911
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode： Normally Black,
8) Pixel Density：257 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	A-Si TFT	-	
Screen Size	3.95	Inch	Diagonal
Resolution	720(W)*3(RGB)*720(H)	Dots	
Interface	3SPI_RGB 18bits	-	40PIN
Module Power Consumption	0.6	Watt	Typ.
VActive VArea	71.93(H) × 71.93(V)	mm	
Pixel pitch (W*H)	0.0999(W)*0.0999(H)	mm	
Module Size (W*H*D) (LCM+CTP)	79.6(W)*85.8(H)*4.10(D)	mm	
Luminance(LCM+CTP)	300	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	TFT (16.7M)/ Transmissive / NB	Colors	

2. ABSOLUTE MAXIMUM RATINGS

(Ta=25℃ VSS=0V)

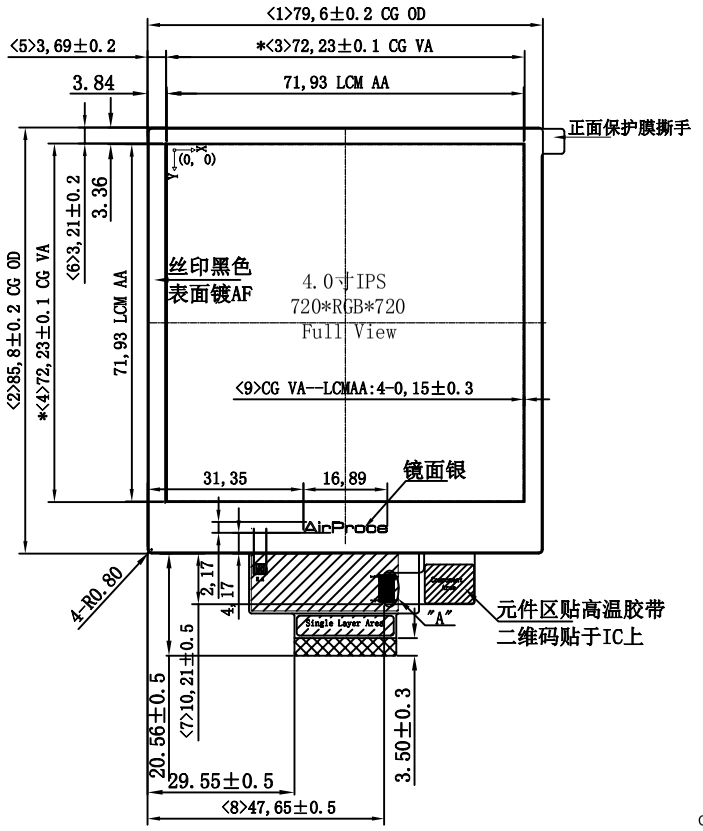
Item	Symbol	Min.	Type	Max.	Unit	Remark
Power Supply Voltage	V_{CI}	-0.3	-	4.5	V	
Logic Input Voltage Range	V_{IH}	-0.3	-	V_{CI} +0.3	V	
Operating Temperature	Topr	-20	-	+70	℃	
Storage Temperature	Tstg	-30	-	+80	℃	

Note1: Absolute maximum rating is the limit value beyond which the IC maybe broken. They do not assure operations.

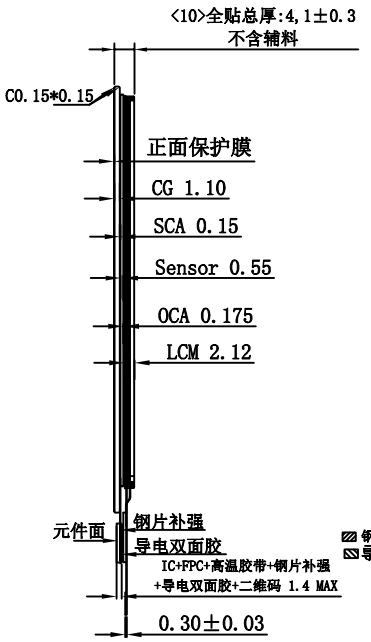
3. MECHANICAL DRAWING

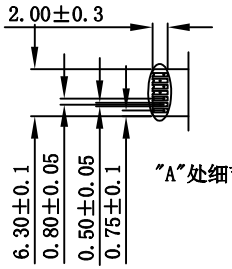
Count drawing & Spec.revision record during discussion with customer		
Rec.	Revision content description	Date
00	FIRST ISSUE	2021-3-18

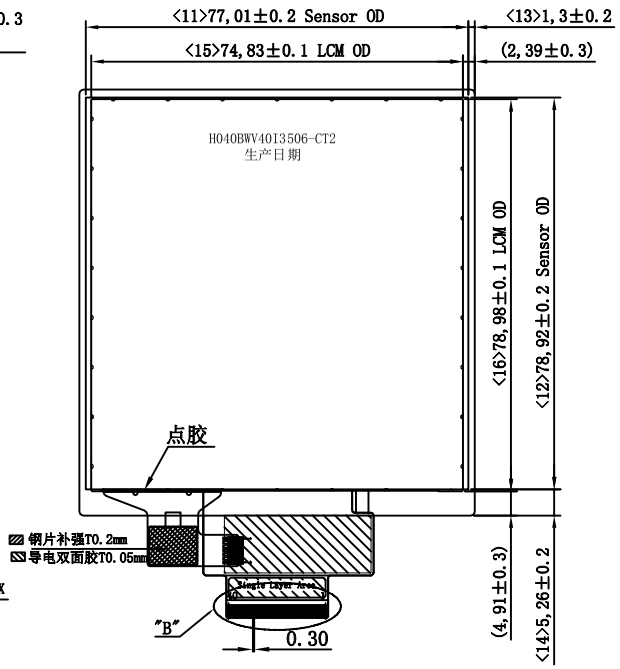
正视图

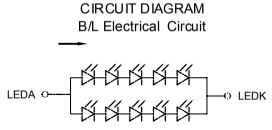


侧视图



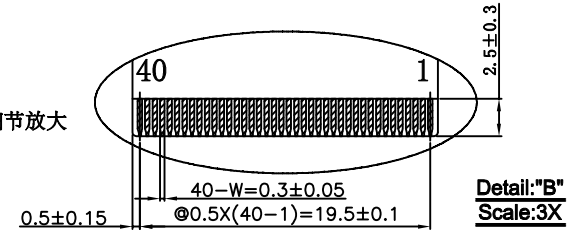






IF=40MA, VF=2.8~3.2

"A"处细节放大



Detail:"B"
Scale:3X

LCD MODULE FPC PIN OUT	
1	LEDA
2	LEDK
3	LEDK
4	GND
5	VCI
6	RESET
7	NC
8	NC
9	SDA
10	SCK
11	CS
12	PCLK
13	DE
14	VSYNC
15	HSYNC
16	DB0
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11
28	DB12
29	DB13
30	DB14
31	DB15
32	DB16
33	DB17
34	TP_GN
35	TP_INT
36	TP_SD
37	TP_SC
38	TP_RES
39	TP_VC
40	TP_GN

CTP PIN ASSIGNMENT		
1	TP_GND	
2	TP_INT	
3	TP_SDA	
4	TP_SCL	
5	TP_RESET	
6	TP_VCI	
7	TP_GND	

Specification:

1.Display mode: 3.95" TFT/ Transmissive / Normally Black
2.Display Color: 16.7M
3.Viewing Direction: Free
4.Controller IC: NV3052C or Compatible
5.Operating temperature: -20°C to +70°C
  Storage temperature: -30°C to +80°C
6.Backlight: 10 chips White LED
7. Unspecified tolerance:±0.30,"( )" reference dimension
8. ROHS compliant

CTP 技术参数：
1.Cover Glass:1.1mm, ITO GLASS:0.55mm;G+G,
2.IC:GT911,通道数RX12*TX12
3.工作电压：3.3V,通讯电压：3.3V
4.透光率≥85%
5.盖板表面硬度要求≥6H;
6.AF要求：表面镀AF
7.工作环境：-20℃~+70℃，≤90%RH
8.储存环境：-30℃~+80℃，≤90%RH
9.◇内尺寸为重点标注尺寸，未注尺寸公差按±0.2mm
10.所有材料须符合☑RoHS ☐包材指令 ☐ REACH ☐ 卤素 ☐ 其它.

INTERFACE	3SPI+RGB Interface	深圳市明瑞光电科技有限公司 Xinrui photoelectric technology (shenzhen) CO.,LTD.	
	FPC Connector	MODEL NAME: TFT Display Module	PART NO.: H040BWV40I3506-CT2
VIEWING DIRECTION	ALL	DWN	REV.: A0 / SHEET OF: 1/1
		CHKD	TOLERANCE UNLESS SPECIFIED: ±0.3
Gray Scale DIRECTION	ALL	PROJECTION: 3RD ANGLE	UNIT: mm / SCALE: 1:1

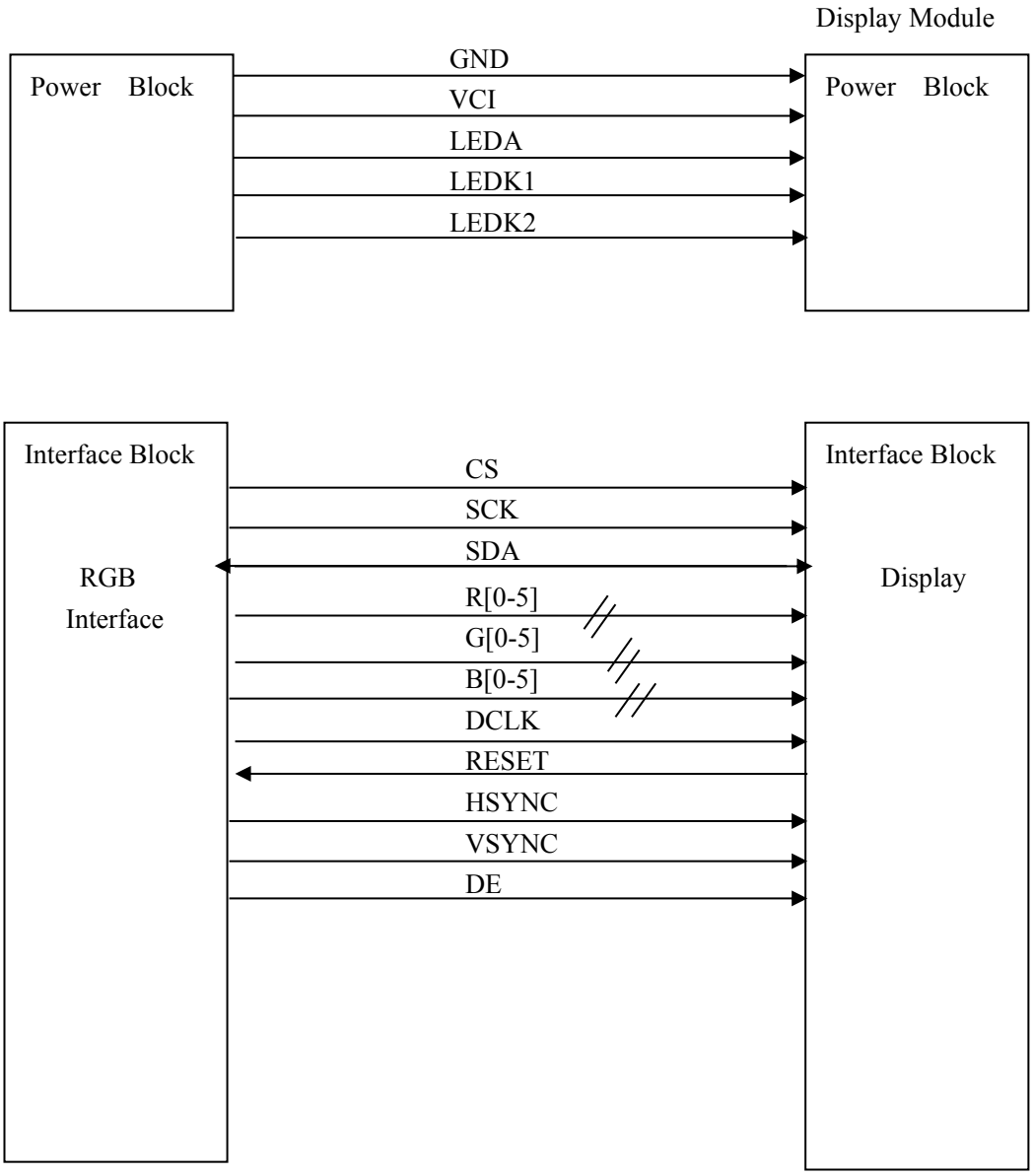
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	LEDA	P	Power supply for backlight anode
2	LEDK1	P	Power supply for backlight cathode
3	LEDK2	P	Power supply for backlight cathode
4	GND	P	Power Ground
5	VCI	P	Power supply to the internal logic power regulator(2.8V)
6	RESET	I	The signal will reset the LCM, Signal is active low.
7-8	NC	-	No conneted
9	SDA	I/O	Serial in/out signal，for initial RGB I/F。
10	SCK	I	serial interface clock，for initial RGB I/F。
11	CS	I	Chip select input pin (“Low” enable)，for initial RGB I/F。
12	PCLK	I	Pixel clock input pin, Negative polarity
13	DE	I	Data input enable. Display access is enabled when DE is “H”
14	VSYNC	I	Vorizontal sync signal, Negative polarity
15	HSYNC	I	Hertical sync signal, Negative polarity
16-21	B0-B5	I	Blue data input.
22-27	G0-G5	I	Green data input.
28-33	R0-R5	I	Red data input.
34	TP_GND	P	Power Ground
35	TP_INT	O	Interrupt signals for TP
36	TP_SDA	I/O	I2C data signals for TP
37	TP_SCL	I	I2C clock signals for TP
38	TP_RST	I	The signal will reset the TP, Signal is active low
34	TP_VCI	P	TP_VDD(2.8V) Power Supply for TP
40	TP_GND	P	Power Ground

4.2 Block Diagram

RGB and Display Module Interface Configuration



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply Voltage	VCI	2.5	2.8	3.3	V	
Power Supply Voltage	-	-	-	-	V	
Power Supply Current	I_{VDD}	-	30	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7VCI	-	VCI	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3VCI	V	-
Panel Power Consumption	P_{VDD}	-	0.099	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.6	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

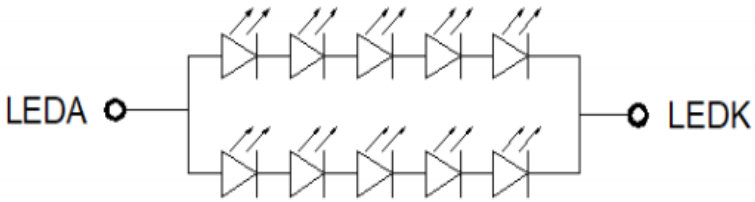
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	14	15	17	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.51	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			10		PCS	

(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module (5 LED Serial, 2 LED Parallel)。
For each LED ： IF=20mA,VF=3.0V(Typ.)/3.4V(Max.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.

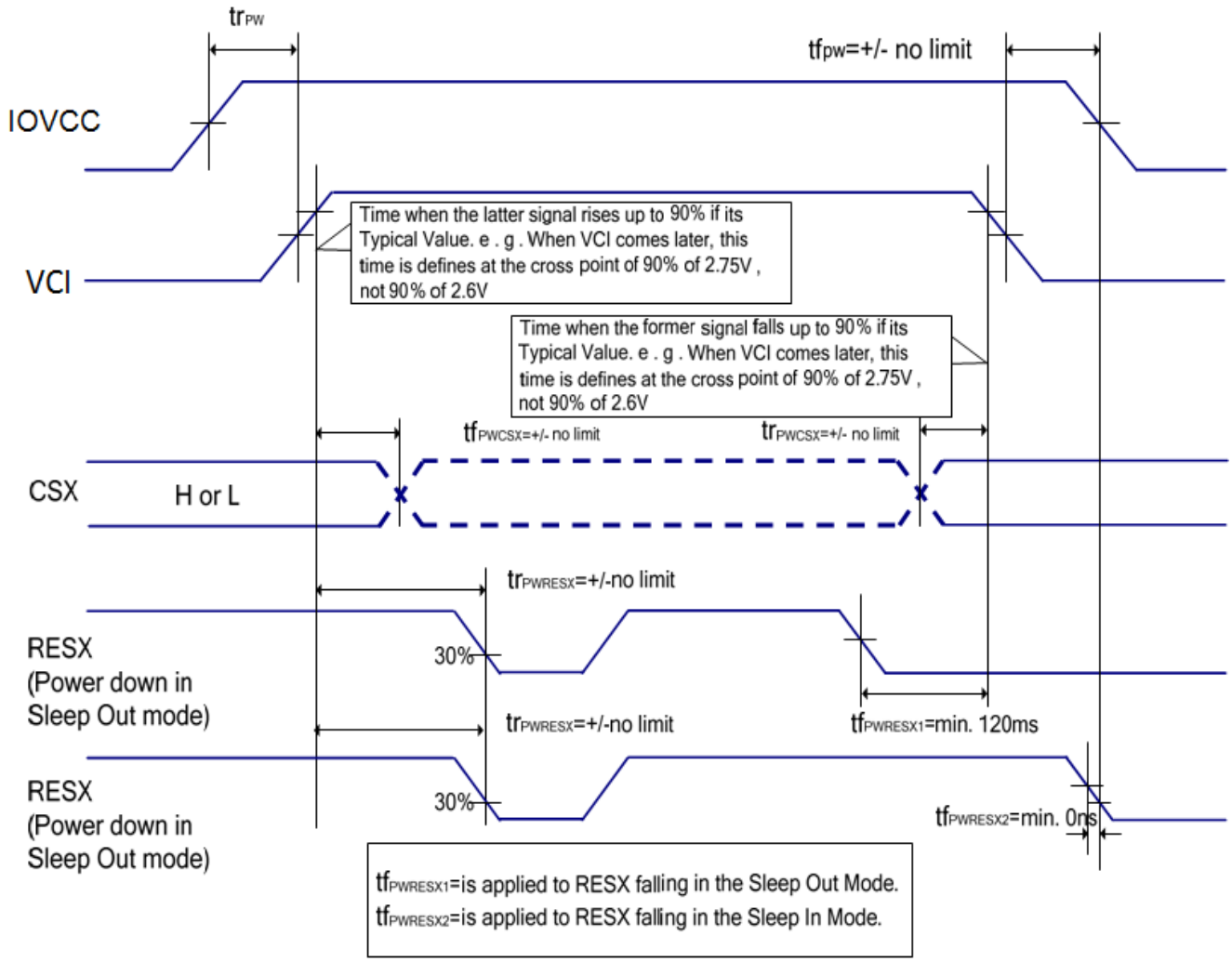


5.3 Power On/Off Sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.
Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.
Also between receiving Sleep In command and Power Off Sequence.
If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
The power on/off sequence is illustrated below:

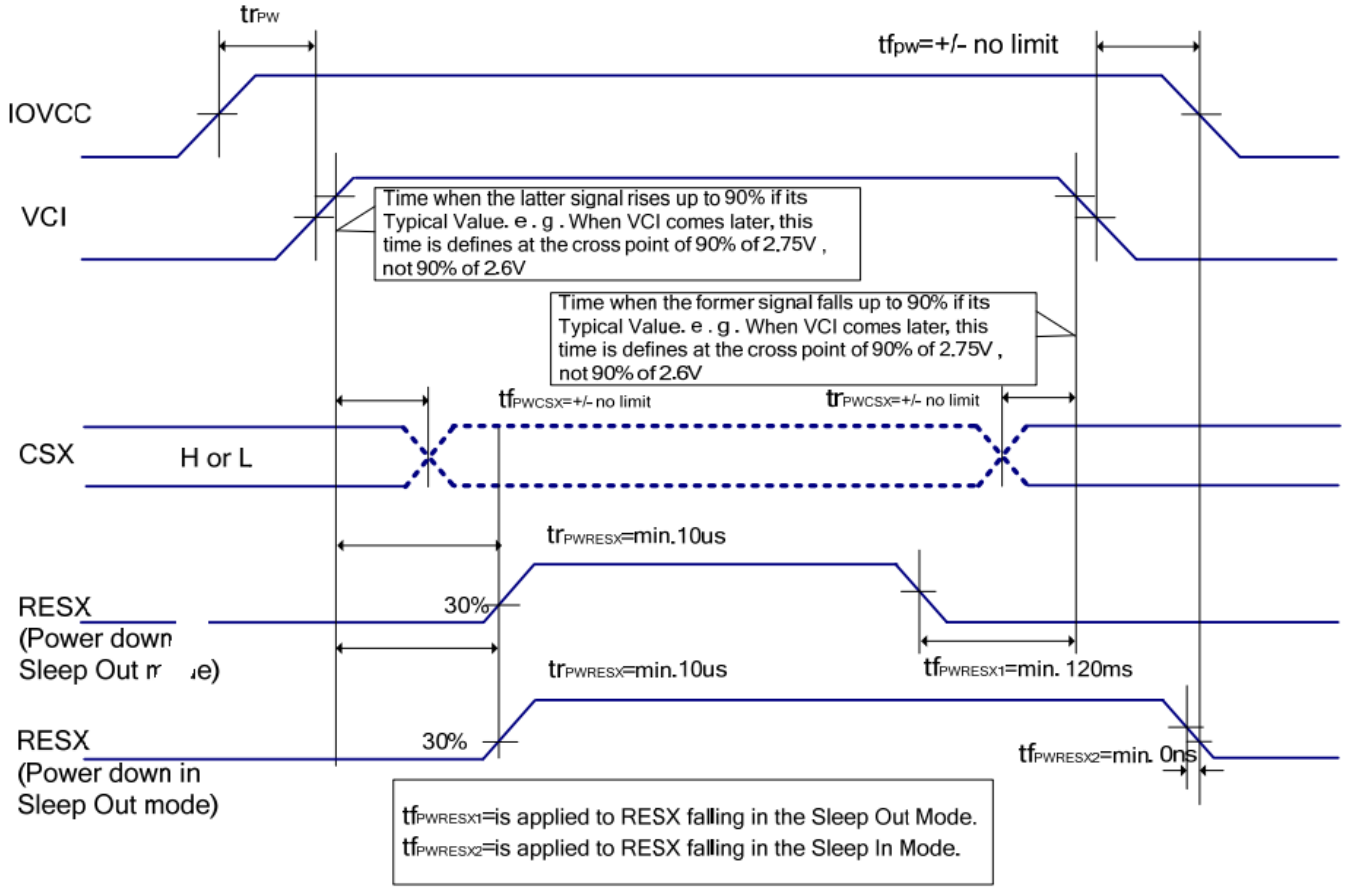
Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed.
There is no timing restriction upon this hardware reset.



Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.4 Timing Characteristics

Timing for 3-Wire SPI Interface

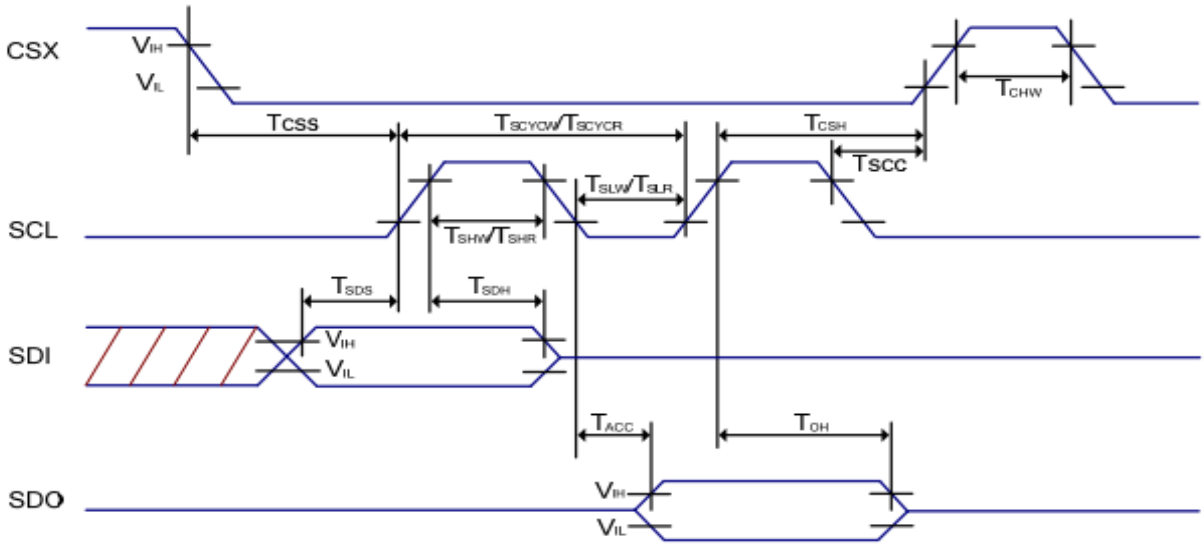


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

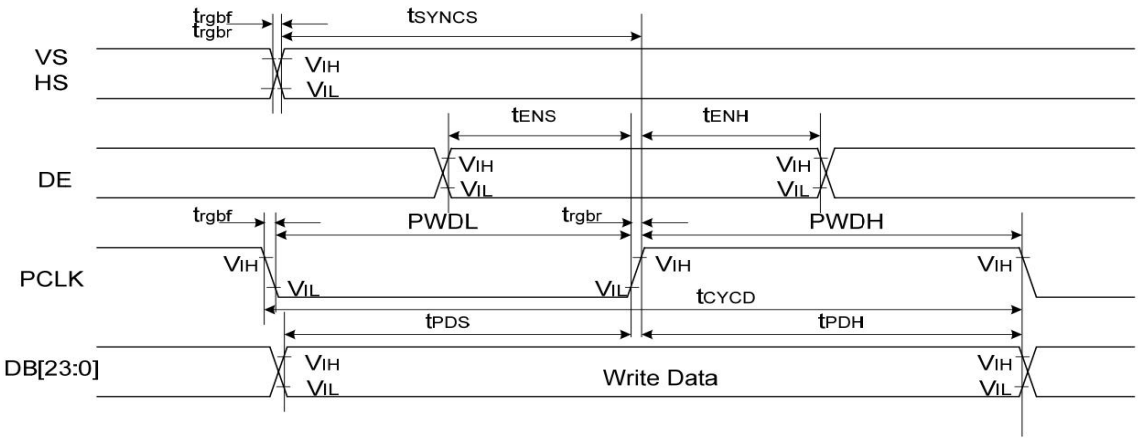
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	-
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip “H” pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T_{SHW}	SCL “H” pulse width (Write)	10	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T_{SHR}	SCL“H” pulse width (Read)	60	-	ns	
	T_{SLR}	SCL“L” pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 70℃

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

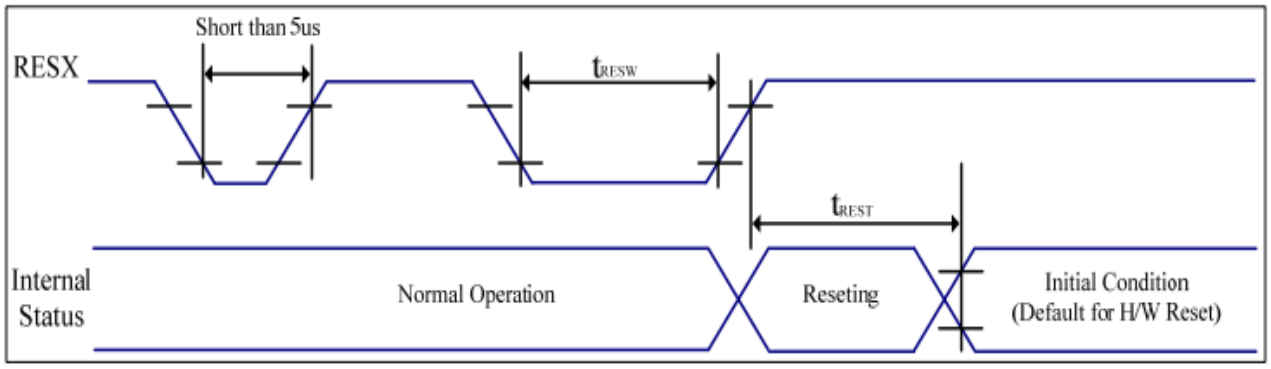
5.5 Timing Diagram

Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

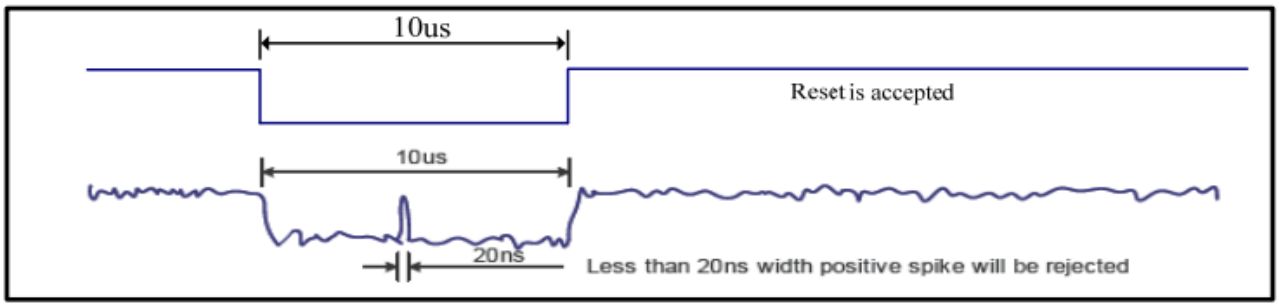
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms..The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

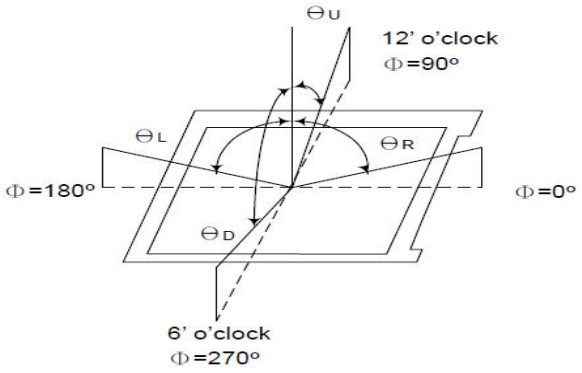
6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	800	1000	-	-	Note(4)
NTSC Ratio	S	θ =0°	63	68	-	%	Note(7)
Luminance	LCM+CTP	θ =0°	-	300	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	-	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	25	35	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	TBD	+0.04	NTSC (x,y)	Note(6)
	W_Y			TBD			
	R_X			TBD			
	R_Y			TBD			
	G_X			TBD			
	G_y			TBD			
	B_X			TBD			
	B_Y			TBD			
Viewing Angle	θ_L	C/R>10	80	85	-	Degree	Note(1)
	θ_R		80	85	-		
	θ_U		80	85	-		
	θ_D		80	85	-		

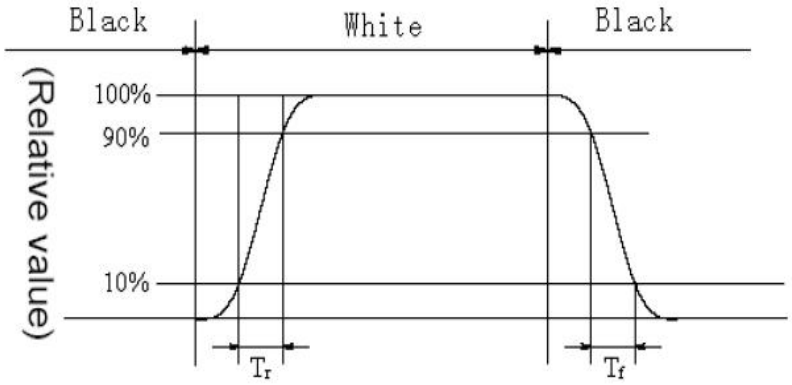
Test Conditions:

1. VDD=2.8V, I_F=40mA (Backlight current), the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

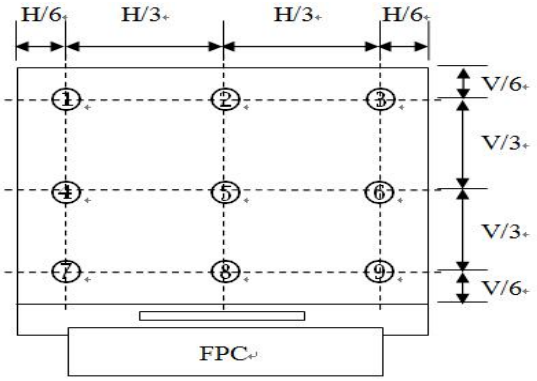


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

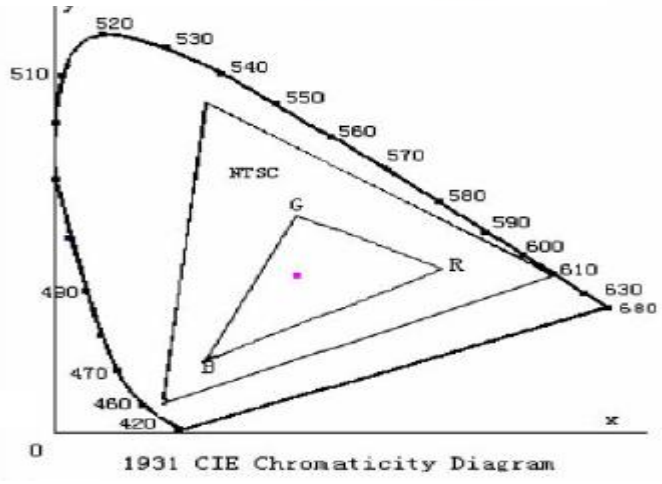
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

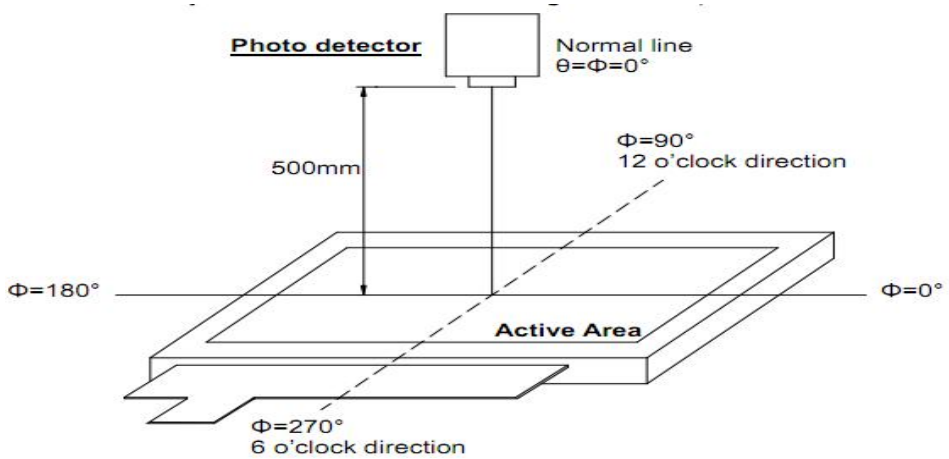
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min ⇆+70°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	80°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2
ESD test	Contact: ±4KV Air: ±8KV	ESD

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

8. PACKAGE DRAWING