深圳市勋瑞光电科技有限公司
Xunrui photoelectric technology （shenzhen）CO,.LTD.

Product Specification

Customer: _____

Model Name: H030BQ45I4003

Date: 2025.03.18

Version: A0

■ **Preliminary Specification**

☐ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

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1. Record of Revision

Rev	Issued Date	Description	Editor
A0	2025/03/18	First Release	LXX

2. General Specifications

Feature		Spec
Characteristics	Size	3.0inch
	Resolution	240(horizontal)*400(Vertical)
	Interface	RGB
	Display Colors	262K
	Technology type	a-Si
	Pixel pitch (mm)	0.1635x 0.1635
	Pixel Configuration	R.G.B.Stripe
	Display Mode	Normally Black
	Driver IC	ST7796PI
	Viewing Direction	ALL
Mechanical	LCM (W x H x D) (mm)	45.04*77.00*2.60
	Active Area(mm)	39.24*65.40
	With /Without TSP	Without
	Weight (g)	-
	LED Numbers	4LEDs

Note 1: Requirements on Environmental Protection: RoHS
Note 2: LCM weight tolerance: +/- 5%

3. Input/output Terminals

PIN NO	PIN NAME	DESCRIPTION
1	IM0	The MCU interface mode select, Please see Note1
2	IM1	
3	IM2	
4	RESET	This signal will reset the device and it must be applied to properly initialize the chip.Signal is active low.
5	VSYNC	Vertical synchronizing input signal for RGB interface operation.
6	HSYNC	Horizontal synchronizing input signal for RGB interface.
7	PCLK	Dot clock signal for RGB interface operation.
8	DE	Data enable signal for RGB interface operation.
9~26	DB17~DB0	In MCU 8080 parallel interface, DB[17:0] are used as data bus: 8-bit I/F: DB[7:0] is used. 9-bit I/F: DB[8:0] is used. 16-bit I/F: DB[15:0] is used. 18-bit I/F: DB[17:0] is used. In RGB interface, DB[17:0] are used as data bus: 16-bit RGB I/F: DB[15:0] are used. 18-bit RGB I/F: DB[17:0] are used.
27	SDO	SPI interface output pin. The data is outputted on the falling edge of the SCL
28	DIN(SDA)	SPI interface input/output pin. The data is latched on the rising edge of the SCL
29	RD	Read enable in 8080 MCU parallel interface. Low-active.
30	WR/SCL	Write enable in MCU parallel interface. In SPI mode, this pin is used as SCL.
31	RS	Display data/command selection pin in MCU interface. RS=’1’: display data or parameter. RS=’0’: register index / command.
32	CS	Chip selection pin. Low-active
33~34	VCC(2.5V~3.3V)	Power supply for analog , booster circuits and I/O system.
35~36	GND	Power Ground.
37~40	LEDK4~LEDK1	Backlight cathode.
41	LEDA	Backlight anode.
42	NC(XR)	Not Connect.
43	NC(YD)	Not Connect.
44	NC(XL)	Not Connect.
45	NC(YU)	Not Connect.

NOTE 1:

-The MCU interface mode select.

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	8080 18-bit Interface	DB[17:0]
0	0	1	8080 9-bit Interface	DB[8:0]
0	1	0	8080 16-bit Interface	DB[15:0]
0	1	1	8080 8-bit Interface	DB[7:0],
1	0	0	Reserve	--
1	0	1	3SPI	SDA, SDO
1	1	0	MIPI	MIPI_DATA MIPI_CLOCK
1	1	1	4Line SPI	SDA, SDO

4. Absolute Maximum Ratings

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{CC}	-0.3	4.6	V	
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

5. Electrical Characteristics

Driving TFT LCD Panel

Ta = 25 °C

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Analog Supply Voltage		V_{CC}	2.5	2.75	3.3	V	
Input Signal Voltage	Low Level	V_{IL}	VSS	-	0.3xV_{CC}	V	
	High Level	V_{IH}	0.7x V_{CC}	-	V_{CC}	V	
Output Signal Voltage	Low Level	V_{OL}	VSS	-	0.2xV_{CC}	V	
	High Level	V_{OH}	0.8x V_{CC}	-	V_{CC}	V	

Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	80		mA	
Forward Voltage	V_F	2.7	3.0	3.3	V	
Backlight Power consumption	W_{BL}	-	240		mW	
LED Lifetime	T	30000	-	-	Hrs	

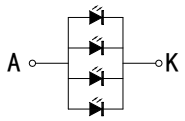
Note 1: Each LED: IF =20 mA, VF =3.0V.

Note 2: Optical performance should be evaluated at Ta=25℃ only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness.

Typical operating life time is estimated data.

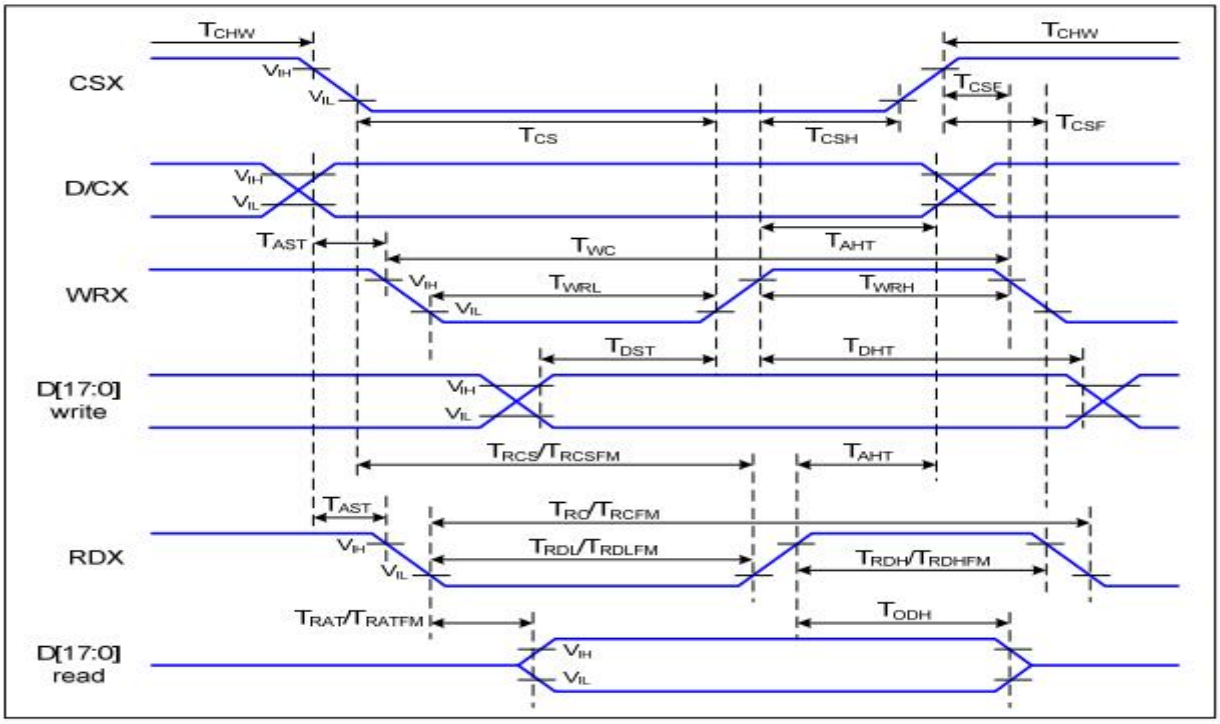
Backlight Circuit Diagram (4*1=4 SMD)



VF=3.0V(TYP), IF=80mA

6. Interface Timing

6.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

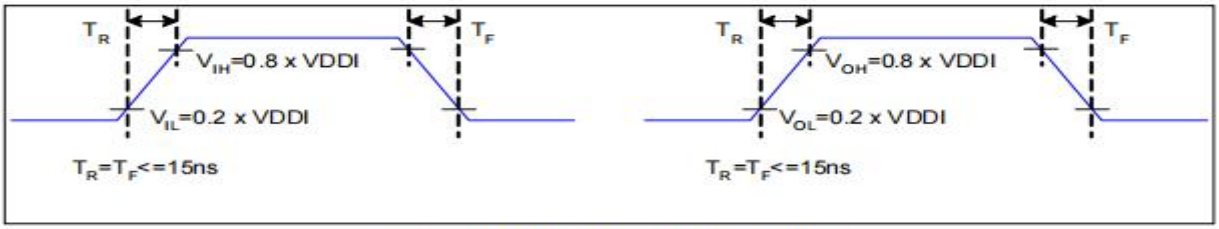


Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

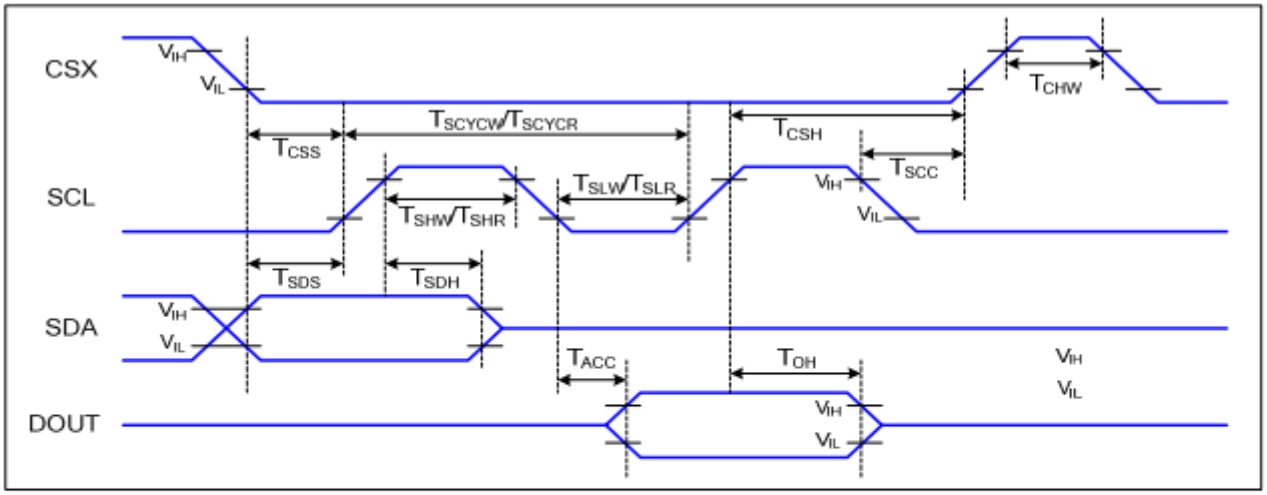
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

6.2 3-SPI Serial Data Transfer Interface Characteristics



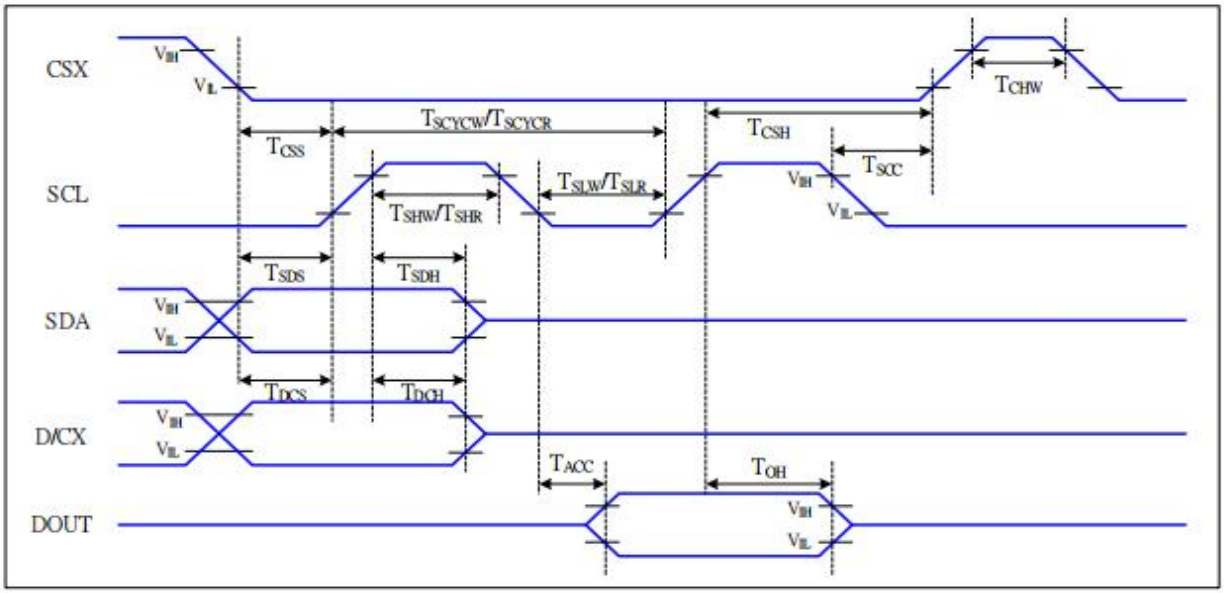
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

6.3 4-SPI Serial Data Transfer Interface Characteristics

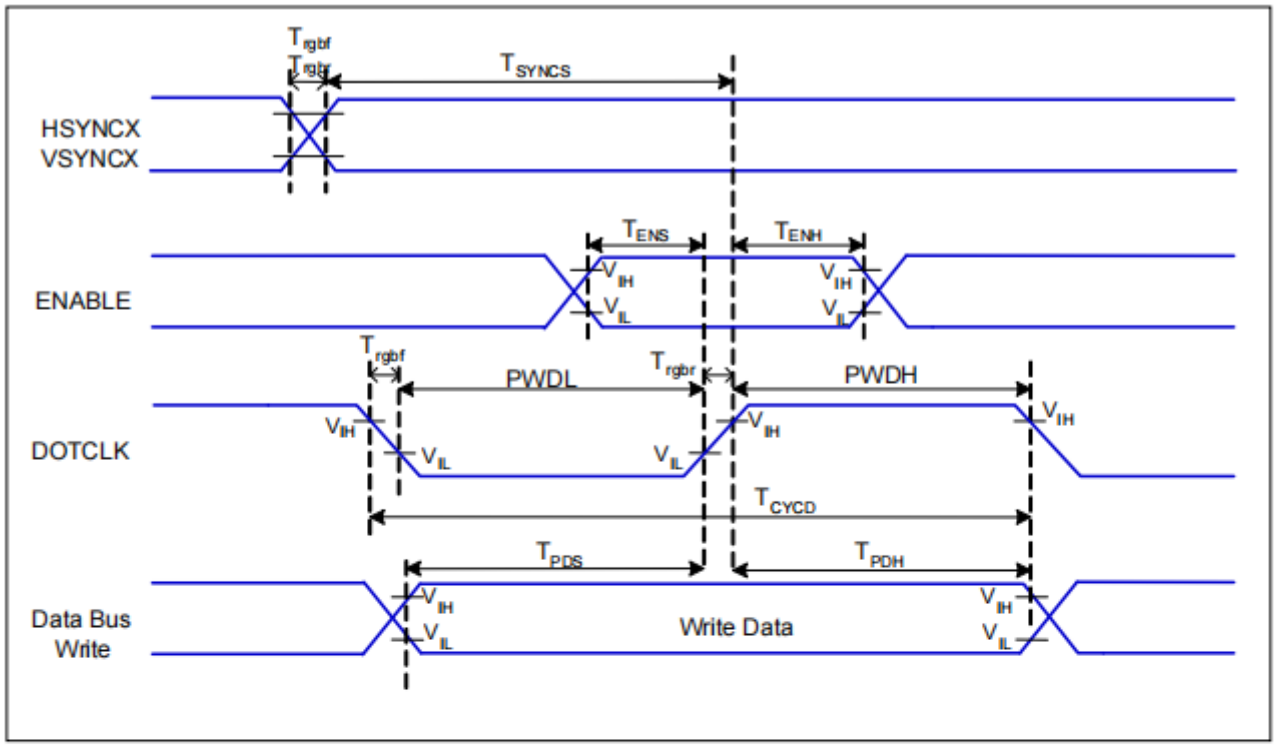


4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

6.4 RGB Interface Characteristics



VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

6.5 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

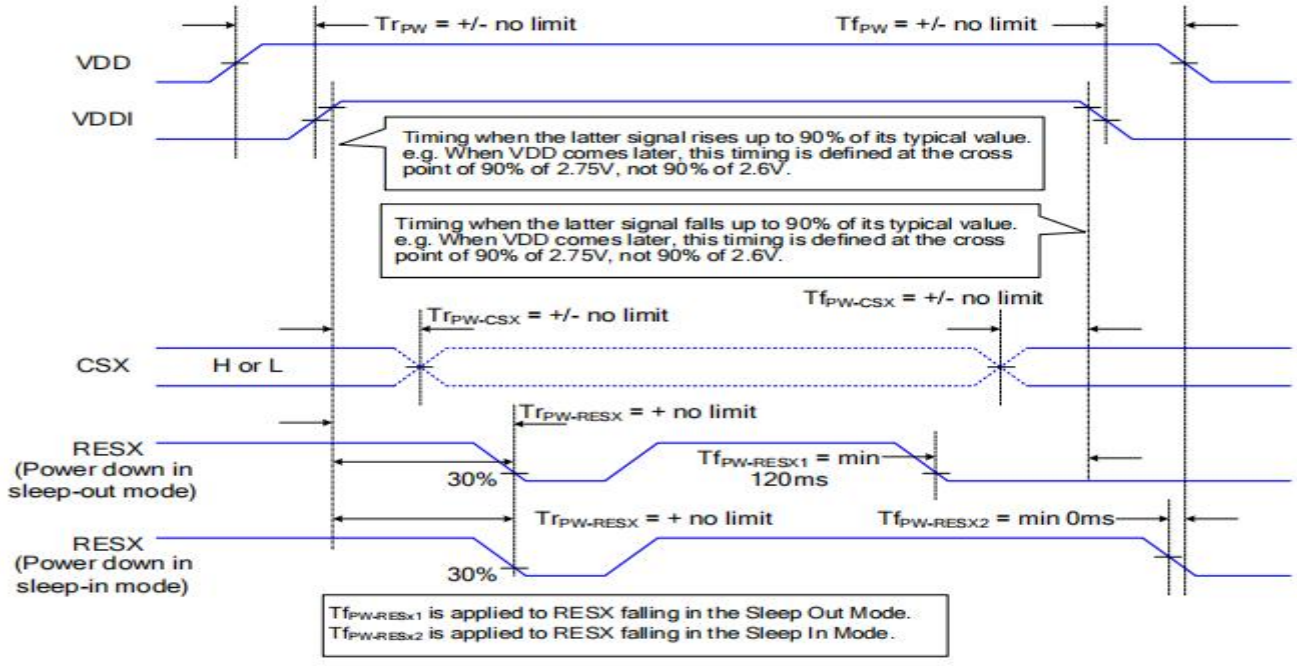
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



6.6 Uncontrolled Power OFF

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up

7. Optical Characteristics

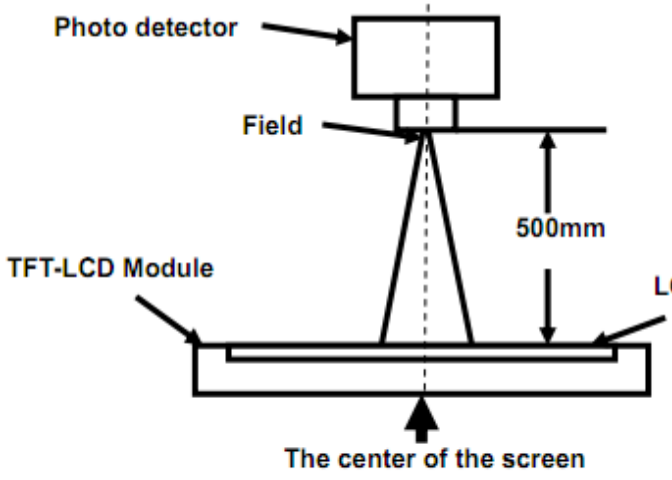
Items		Symbol	Condition	Min	Typ	Max	Unit		Remark
Viewing angles		θ_T	Center CR≥10	80	85	-	Degree		Note2
		θ_B		80	85	-			
		θ_L		80	85	-			
		θ_R		80	85	-			
Contrast Ratio		CR	Θ =0	600	800	-	-		Note1, Note3
Response Time		$T_{ON}+T_{OFF}$	25°C	-	25	35	ms		Note1, Note4
Chromaticity	White	X_W	Backlight is on	0.280	0.310	0.340	-		Note1, Note5
		Y_W		0.281	0.311	0.341	-		
Uniformity		U		80	-	-	%		Note1, Note6
NTSC				60	70	-	%		Note5
Luminance		L		400	450	-	nits		Note1, Note7

Test Conditions:

1. IF= 20mA (one channel), the ambient temperature is 25.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.
Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).

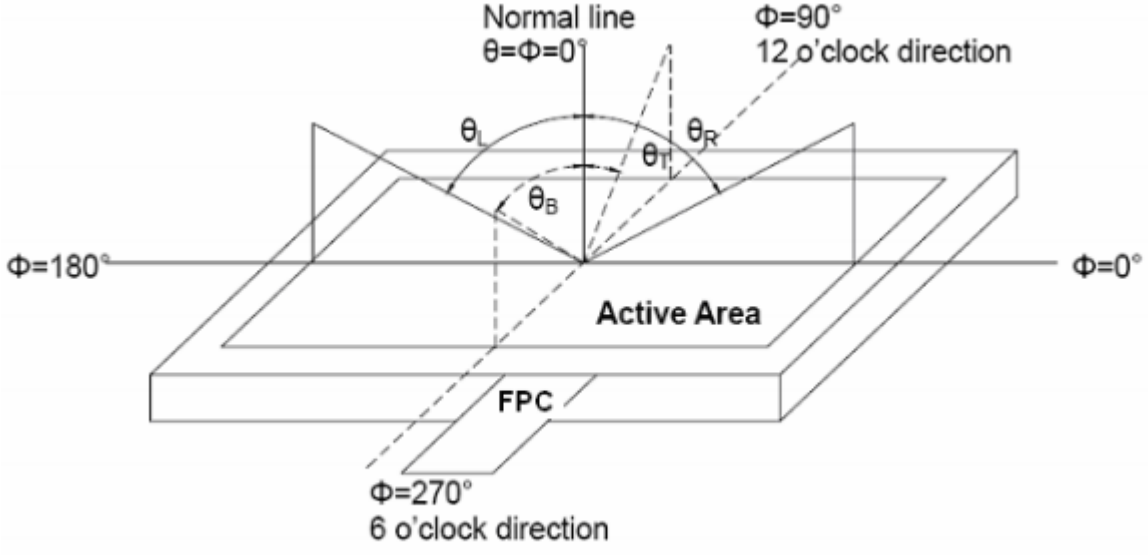


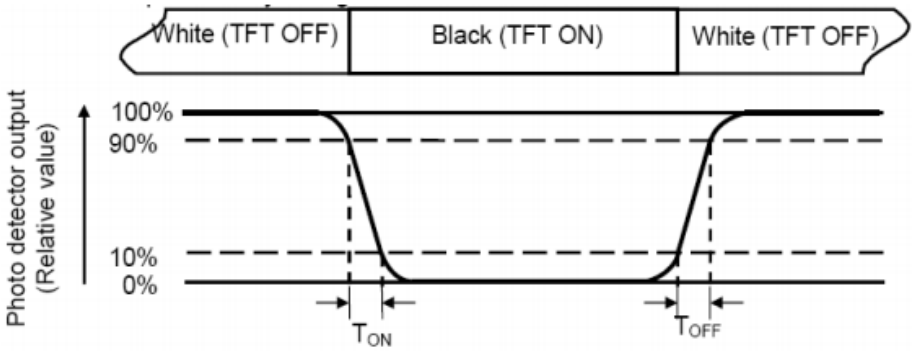
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between “White” state

and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931).

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width

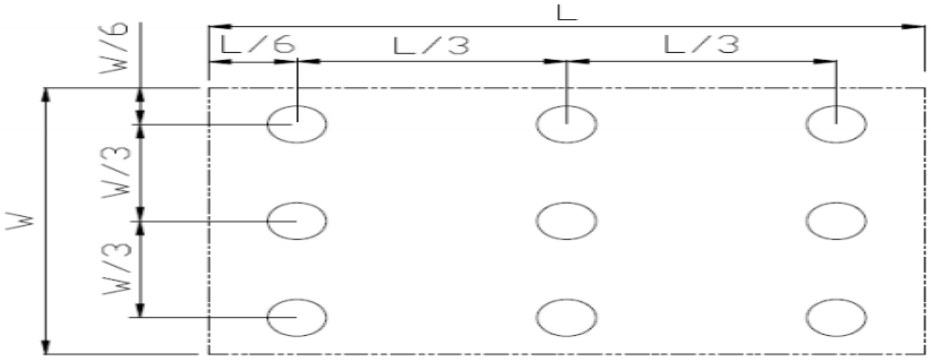


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

8. Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 120hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 120hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 120hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 120hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5times; (Environment: 15℃ ~35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z,3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. TS is the temperature of panel's surface.
Note: 2. Ta is the ambient temperature of sample.

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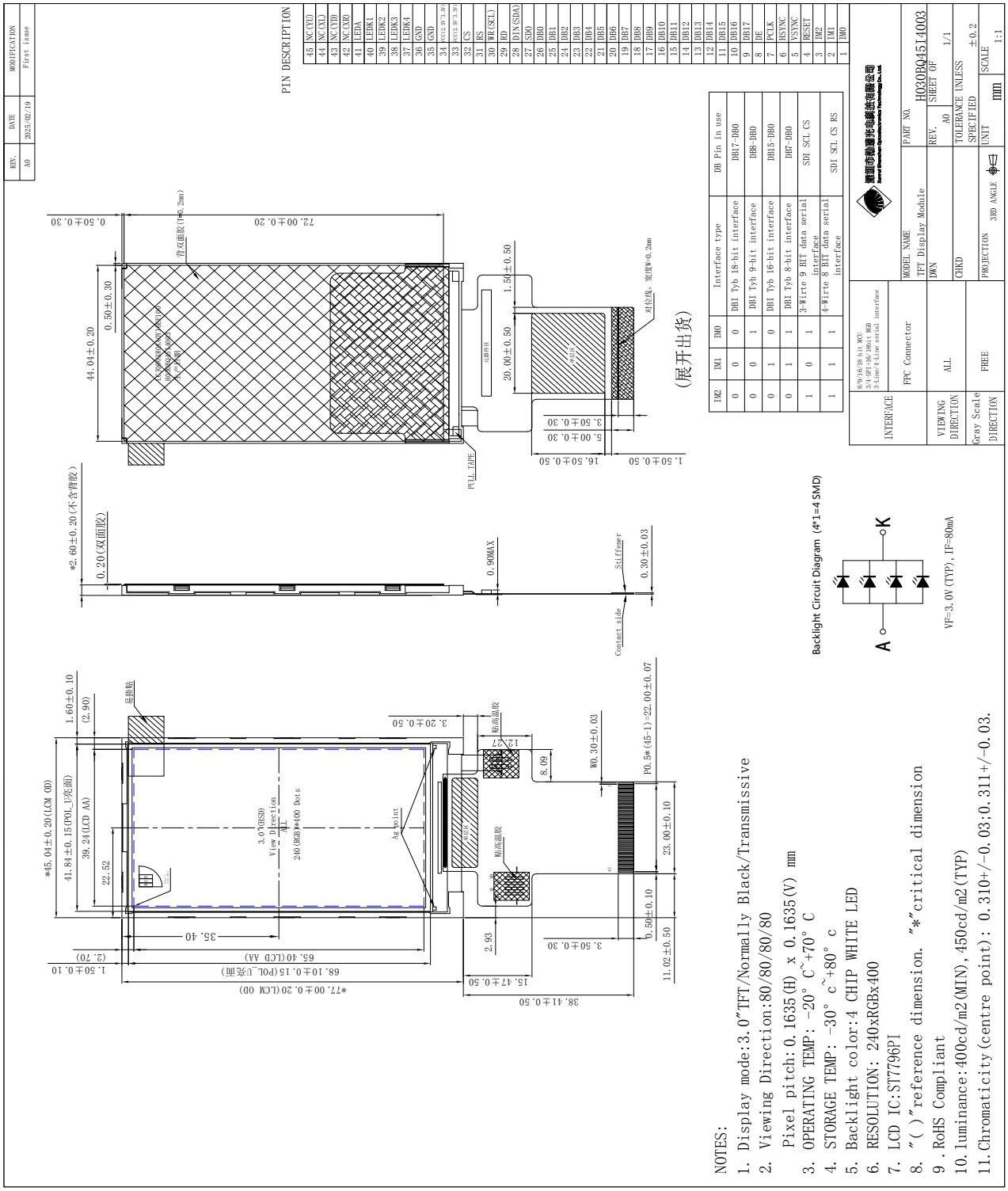
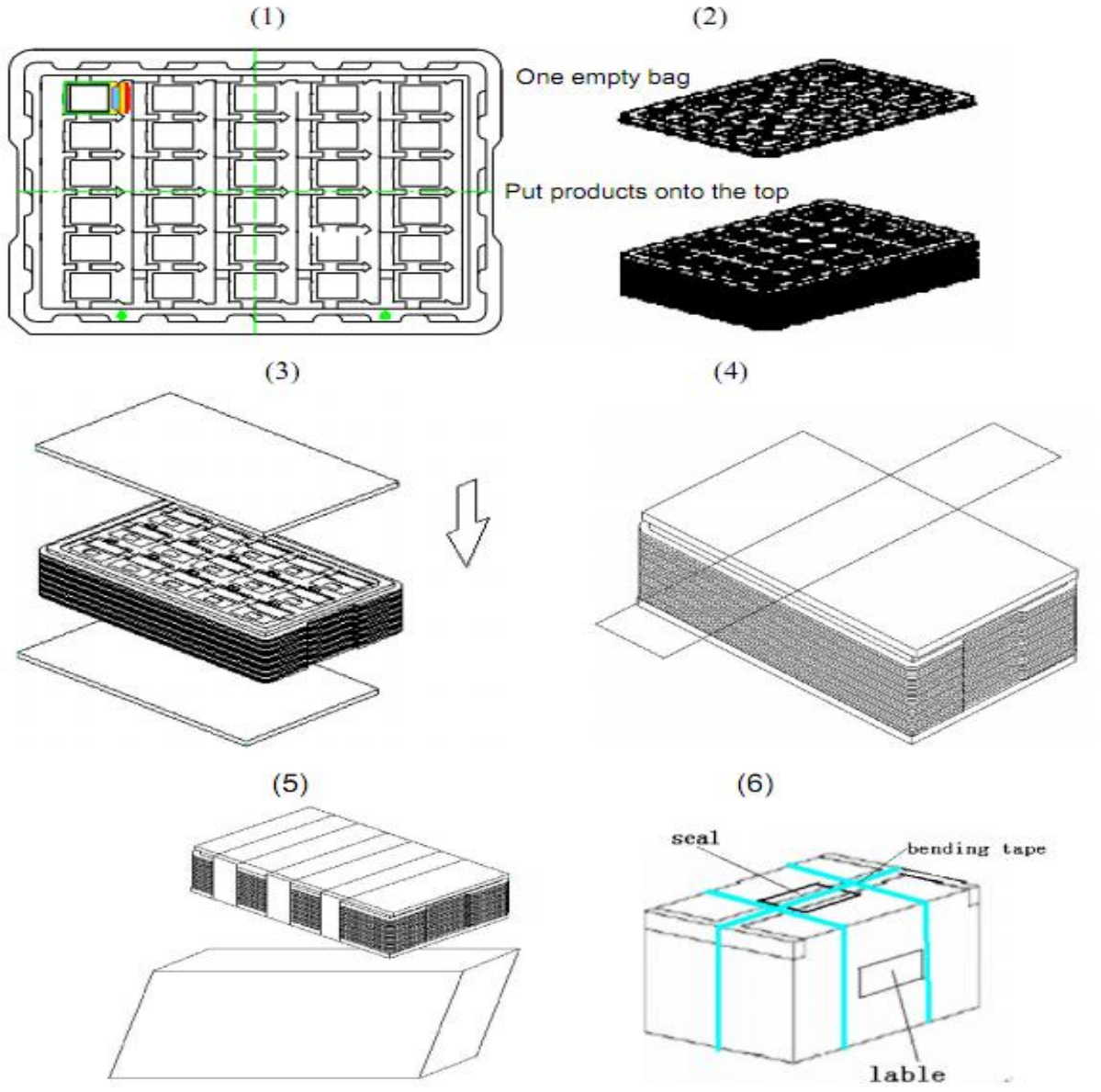
9. Mechanical Drawing



10. Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
-Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1 Be sure to ground the body when handling the LCD Modules.

11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.