深圳市勋瑞光电科技有限公司
Xunrui Shenzhen Optoelectronics Technology Co., Ltd.

CERT. No. QAC0946535 (ISO9001)   CERT. No. HKG002005 (ISO14001)

Product Specification

Customer: _____

Model Name: _____H024HQ40E2543_____

Date: _____

Version: _____

■ **Preliminary Specification**

☐ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

TABLE OF Contents

1.General Description

H024HQ40E2543 is a 240RGB*320 dots matrix TFT LCD module. It has a TFT panel composed of 240 sources and 320gates. The LCM can be easily accessed by micro-controller.
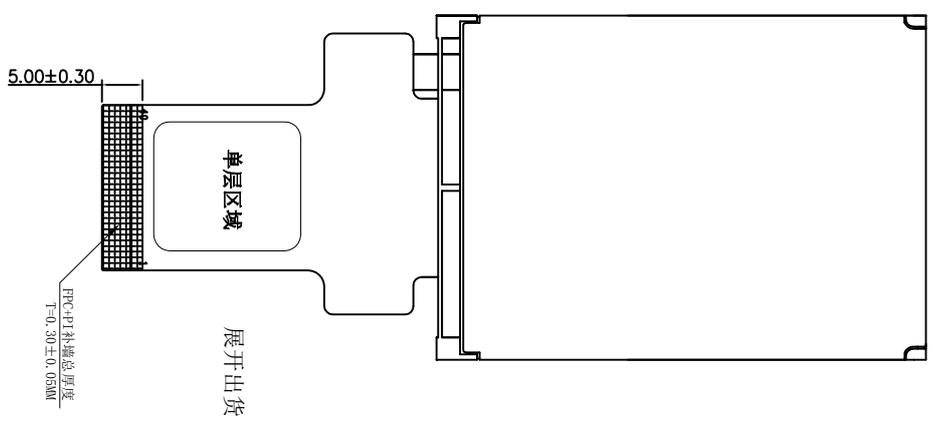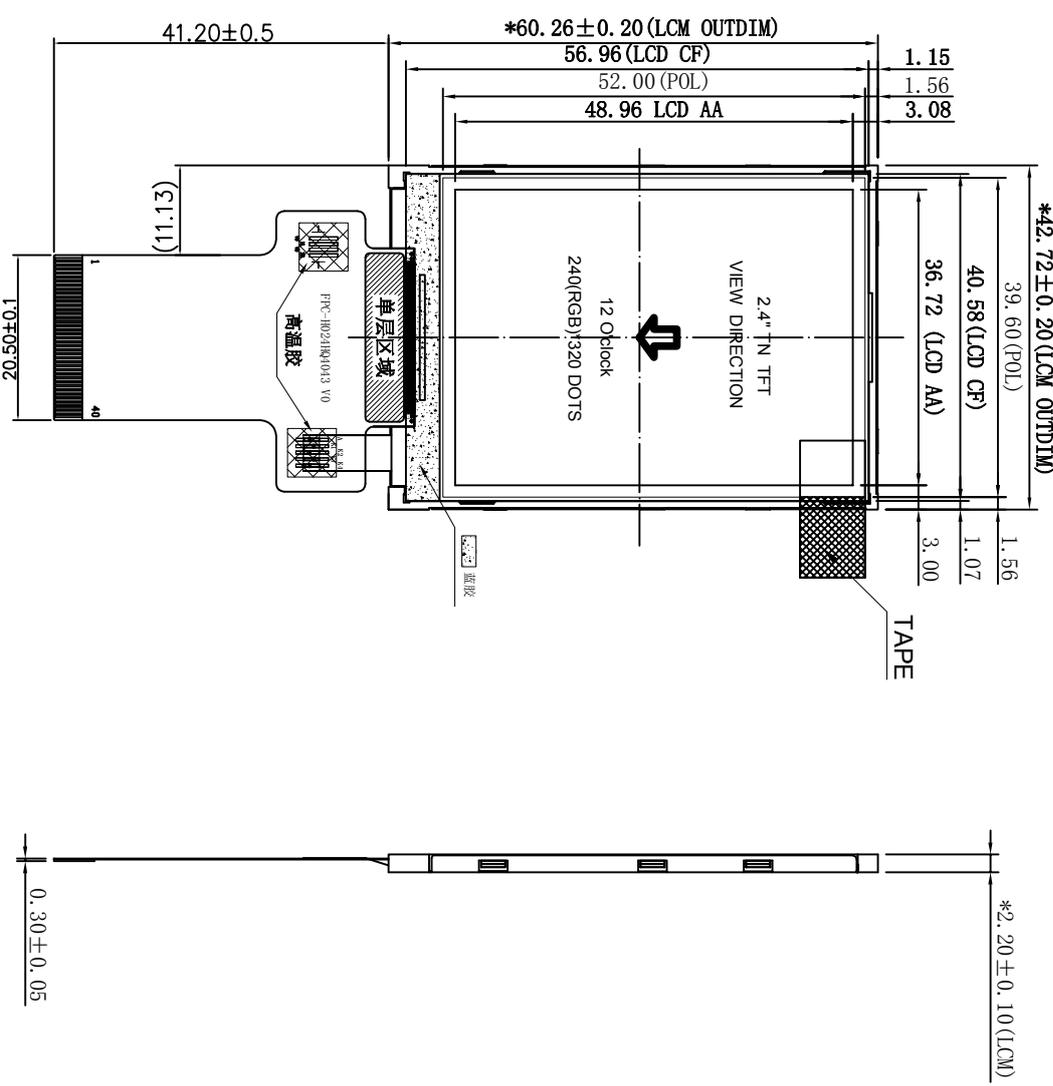
2. Features

Display Mode	Transmissive
	a-TFT
Display Format	Graphic 240RGB*320 Dot-matrix
Input Data	3 线串口/4 线串口/8bits /16bits parallel interface
Viewing Direction	12 o'clock
Drive	ST7789V

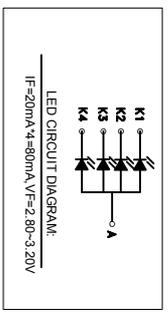## 3. Mechanical Specification

Item	Specifications	Unit
Dimensional outline	42.72(W)*60.26(H)*2.20+/-0.1 (T) (FPC not include)	mm
Resolution	240RGB*320	dots
LCD Active area	36.72(W)*48.96(H)	mm
Pixel size	0.180(W)*0.180(H)	mm

4. Mechanical Dimension

NOTES:
1. DISPLAY TYPE: 2.4 INCH TFT /TRANSMISSIVE
2. BACKLIGHT: 4 CHIP WHITE LED, IN PARALLEL
3. OPERATING TEMP: -20°C~+70°C
4. STORAGE TEMP: -30°C~+80°C
5. RESOLUTION: 240RGBx320 DOTS
6. LCD IC:ST7789V
7. Luminance:250cd/m2
8. "( )"reference dimension. "*"critical dimension
9. RoHS Compliant

LED CIRCUIT DIAGRAM:
IF=20mA*4=80mA,VF=2.80~3.20V
K1 K2 K3 K4
A

41.20±0.5
*60.26±0.20(LCM OUTDIM)
56.96(LCD CF)
52.00(POL)
48.96 LCD AA
1.15
1.56
3.08
*42.72±0.20(LCM OUTDIM)
39.60(POL)
40.58(LCD CF)
36.72 (LCD AA)

2.4" TN TFT
VIEW DIRECTION
12 O'clock
240(RGB)320 DOTS

1.56
1.07
3.00
20±0.1
(11.1 3)
TAPE

FPC-H024HQ41043 V0
单层区域
高温胶
蓝胶

0.30±0.05
*2.20±0.10(LCM)

5.00±0.30
单层区域
展开出货
FPC+PI补强总厚度
T=0.30±0.05MM

INTERFACE	MCU Interface
	FPC welding
VIEWING DIRECTION	6 O'clock
Gray Scale DIRECTION	12 O'clock

MODEL NAME	TFT Display Module		
PART NO.	H024HQ40E2543		
REV.	1.0	SHEET OF	1/1
DWN	gl.Liu	TOLERANCE UNLESS SPECIFIED	
CHKD	gl.Liu		
PROJECTION	3RD ANGLE	UNIT	mm
		SCALE	1:1
			±0.3

PIN	SYMBOL
1	X(L)
2	Y(U)
3	X(R)
4	Y(D)
5	GND
6	IOVCC
7	VCI
8	FMARK
9	CS
10	RS/SCL/
11	WR/A0
12	RD
13	SPI_SDI
14	SPI_SD
15	RESET
16	GND
17	DB0
18	DB1
19	DB2
20	DB3
21	DB4
22	DB5
23	DB6
24	DB7
25	DB8
26	DB9
27	DB1C
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	A
34	K
35	K
36	K
37	GND
38	IM0
39	IM1
40	IM2

1.0
2021.03.02
First issue

5. Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Supply voltage	V	-0.3	4.6	V	
Operating temperature	V_T	-0.3	Vcc+0.3	V	
Storage temperature	T_{OPR}	-20	70	℃	
Storage temperature	T_{STR}	-30	80	℃	

6.   Electrical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Logic	V_{CC}		2.7	2.8	3.3	V
Input Voltage	H level	T_{IH}		0.8*IOVCC		IOVCC	V
	L level	T_{IL}		-0.3		0.2* IOVCC	
Storage temperature		I_{DD}	With internal voltage generation V_{CC}=2.8V; T_{emp}=25℃			TBD	mA

7. Backlight Characteristic

Item	Symbol	Min	Typical	Max	Unit
LED module Forward voltage	V_{LED}	3.0	3.2	3.4	V
LED module current	V_{LED}		80		mA
L/G Surface Luminance ★1	L_S	3000			Cd/m^3
LCM Surface brightness uniform ★2	L_D	80			%

★ 1Test condition is:
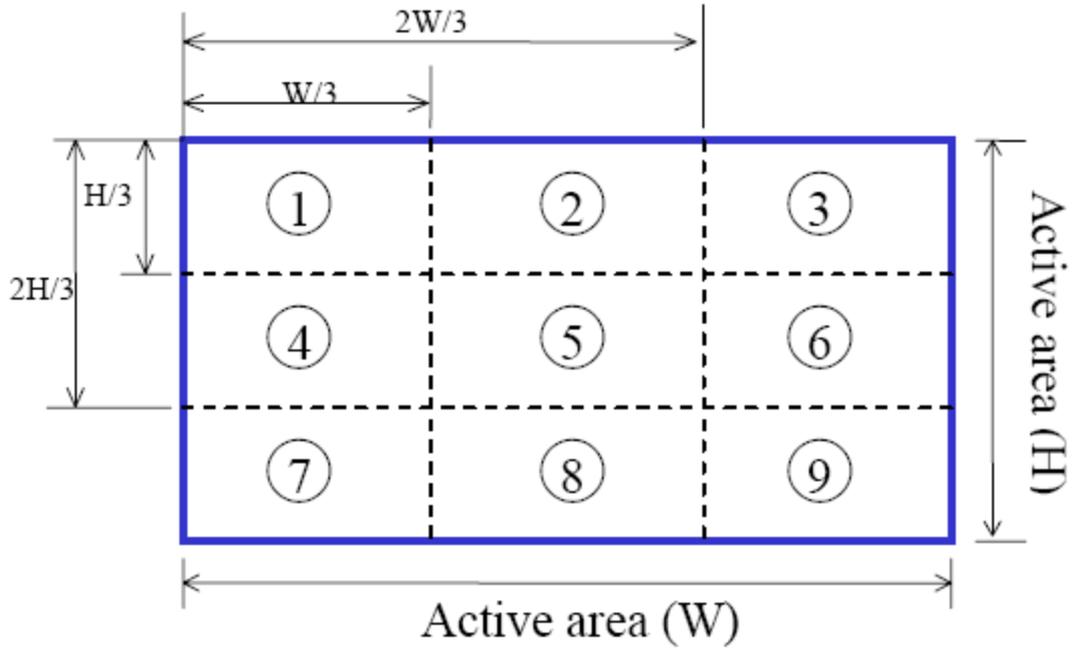
(a) Center point on active area.

(b)Best Contrast.

★2Uniform measure condition:

(1)Measure 9 point. Measure location show below;

(2)Uniform=(Min. brightness /Max. brightness)*100%

(3)Best Contrast.

8. Module Function Description

8.1 Pin Descriptions

PIN No.	Symbol	Description
1	X(L)	Touch panel control pin （触摸屏控制脚）
2	Y(U)	Touch panel control pin （触摸屏控制脚）
3	X(R)	Touch panel control pin （触摸屏控制脚）
4	Y(D)	Touch panel control pin （触摸屏控制脚）
5	GND	Ground （接地脚）
6	IOVCC	Power supply for LCM（2.8V-3.3V） （屏供电脚）
7	VCI	Power supply for LCM（2.8V-3.3V） （屏供电脚）
8	FMARK	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin. （帧同信号,不用时悬空）
9	CS/SPI CS	Chip select pin ("Low" enable) （屏驱动芯片片选脚，低电平有效）
10	RS/SPI SCL/SCK	This pin is used to select "Data or Command" in the parallel interface or serial data interface. (用于并口或者串口) Parallel(并口): When RS= '1', data is selected.(选择数据) When RS= '0', command is selected.(选择寄存器) Serial(串口): This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. (3线串口或者4线串口的时钟信号) If not used, this pin should be connected to IOVCC or GND.

		(不用时接 IOVCC 或者接地)
11	WR/A0(4 线)	Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. *Fix to IOVCC level when not in use.* （并口的写控制脚或者 4 线串口的寄存器/数据选择，不用时接 IOVCC）
12	RD	Serves as a read signal and MCU read data at the rising edge. *Fix to IOVCC level when not in use.* （并口的读控制脚,不用时接 IOVCC）
13	SPI SDI/SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND （串口数据输入信号,不用时接 IOVCC 或者接地）
14	SPI SDO	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin （串口数据输出信号，不用时悬空）
15	RESET	LCM Reset pin Signal is active low. （屏复位脚,低电平复位）
16	GND	Ground （接地脚）
17-24	DB0-DB7	Data bus *Fix to GND level when not in use* (低 8 位数据线,不用时接地)
25-32	DB8-DB15	Data bus *Fix to GND level when not in use* (高 8 位数据线,不用时接地)
33	A	Anode of Backlight (3.0V-3.4V Typical:3.2V) （背光正极供电脚,电压范围:3.0-3.4V,典型值:3.2V）
34-36	K	Cathode of Backlight （背光负极供电脚）
37	GND	Ground （接地脚）

38	IM0	Select the MCU interface mode (接口选择)
39	IM1	
40	IM2	

IM2 IM1 IM0

IM2	IM1	IM0			
0	0	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1]
0	0	1	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10]
0	1	0	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
0	1	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]
1	0	1	3-wire 9-bit data serial interface Ⅱ	SDI: In SDO: Out	
1	1	0	4-wire 8-bit data serial interface Ⅱ	SDI: In SDO: Out	

NOTE：
D[8:1]即低 8 位数据线 DB7-DB0D
D[17:10]即高 8 位数据线 DB15-DB8

关于供电说明：

IOVCC 和 **VCC** 连一起，用 **2.8V-3.3V** 供电；背光 **LED** 可以单独供电（**3.0-3.4 V**），也可以和 **VCC** 共用一组电压（**A** 为正接 **VCC**，**K** 连一起作为负接地）.

8.2 Timing characteristics.

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus
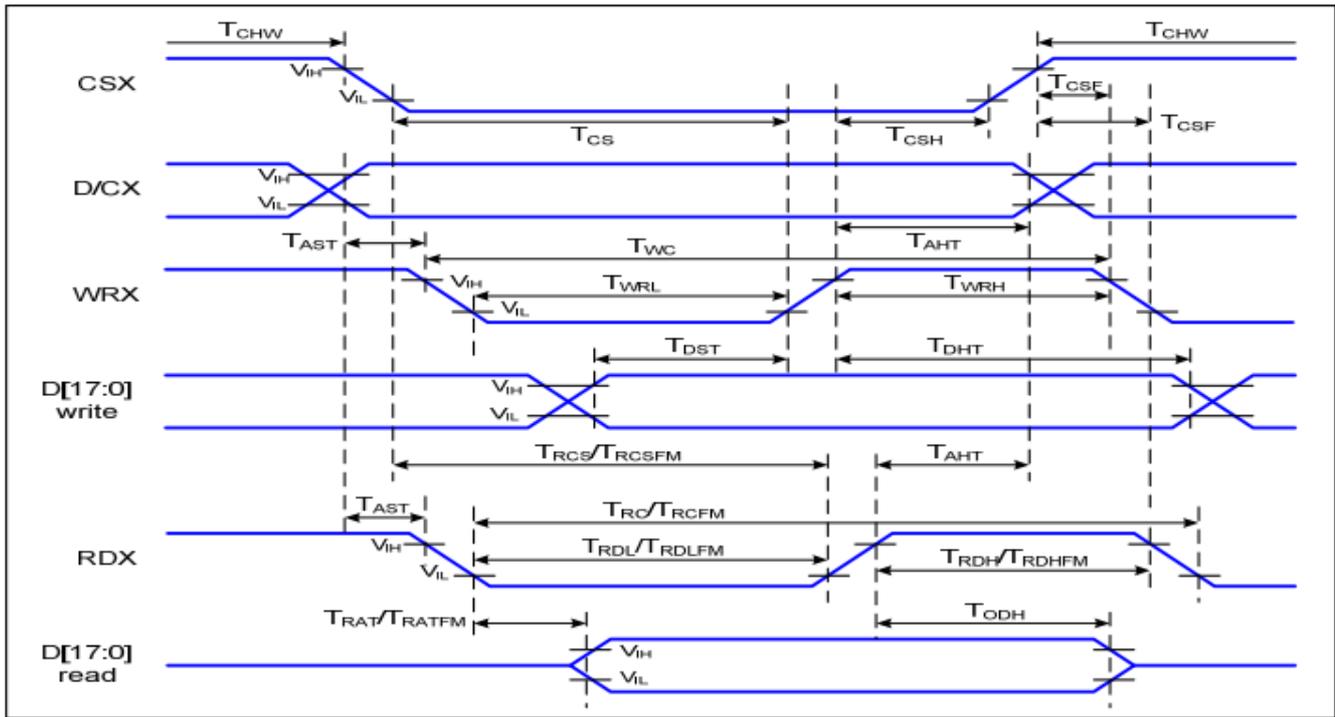
Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

$VDDI=1.65$ to $3.3V$, $VDD=2.4$ to $3.3V$, $AGND=DGND=0V$, $Ta=25℃$

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

T_{DHT}	Data hold time	10		ns	
T_{RAT}	Read access time (ID)		40	ns	
T_{RATFM}	Read access time (FM)		340	ns	
T_{ODH}	Output disable time	20	80	ns	

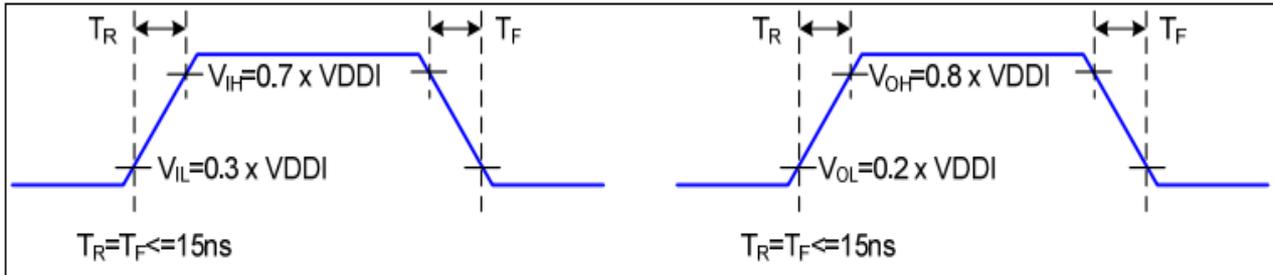**Table 4 8080 Parallel Interface Characteristics**
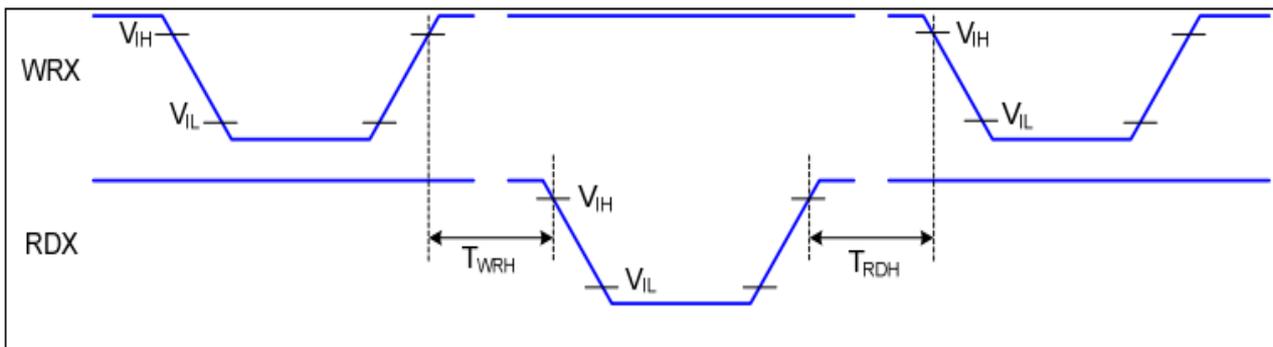

Figure 2 Rising and Falling Timing for I/O Signal

Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

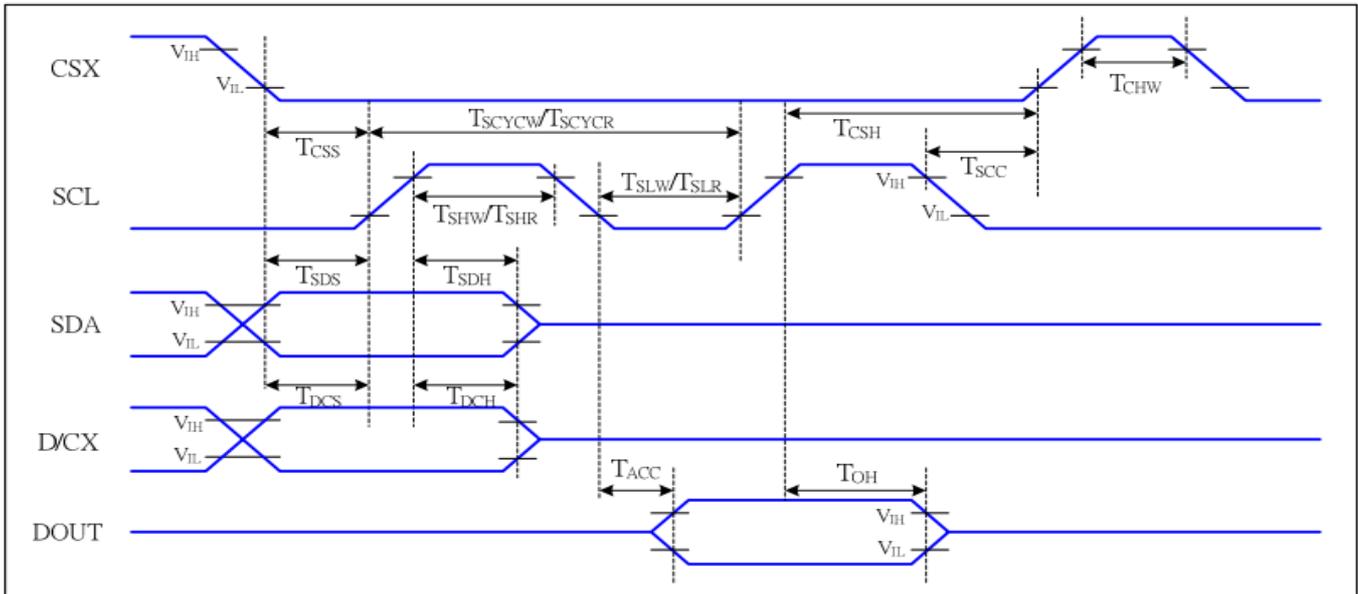### 7.4.2 Serial Interface Characteristics (3-line serial):
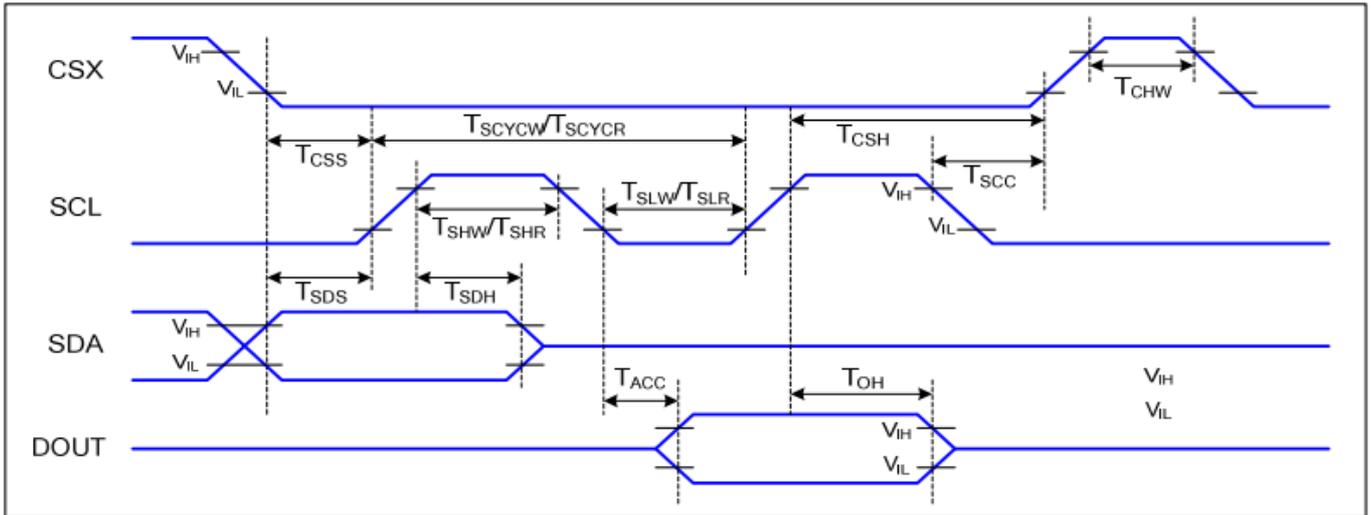
Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.3 Serial Interface Characteristics (4-line serial):

Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9.Electro-optical Characteristics

Item	Symbol	Conditions	Temp	Min.	Typ.	Max.	Unit	Note
Response Time	T_R	$\theta = \phi = 0$	25℃		TBD	TBD	msec	NOTE2
	T_F				TBD	TBD		
Viewing Angle Range	$\phi=0^0$（6"）	$\phi=90^0$（3"）	$\phi=180^0$（12"）			$\phi=270^0$（9"）		NOTE3
θ（25℃）CR≥10	TBD	TBD	TBD			TBD		NOTE3

The above "viewing angle" is the measuring position with the largest contrast ratio. Not for good image quality. Viewing direction for good image quality is 12 O'clock.

●For panel only

●Electro-Optical Characteristics Test Method
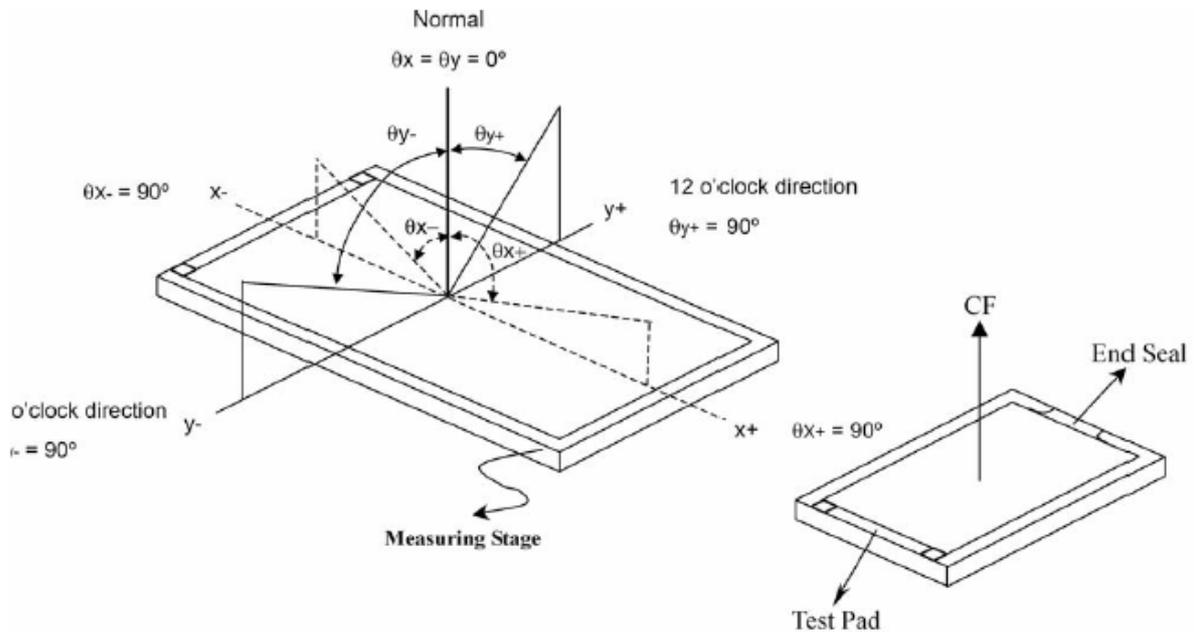
$$Vop = (V_{10, ON} + V_{90, OFF})/2$$
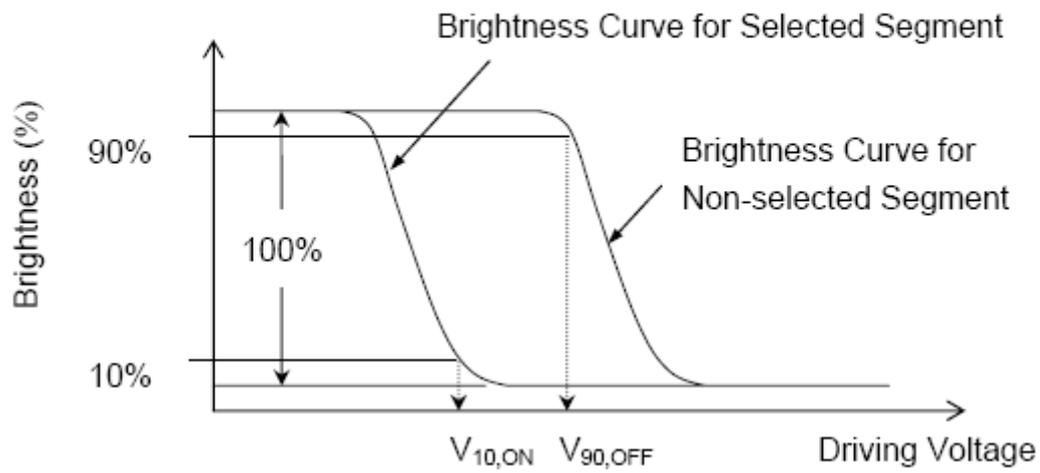
.Note2.Definition of Optical Response Time:
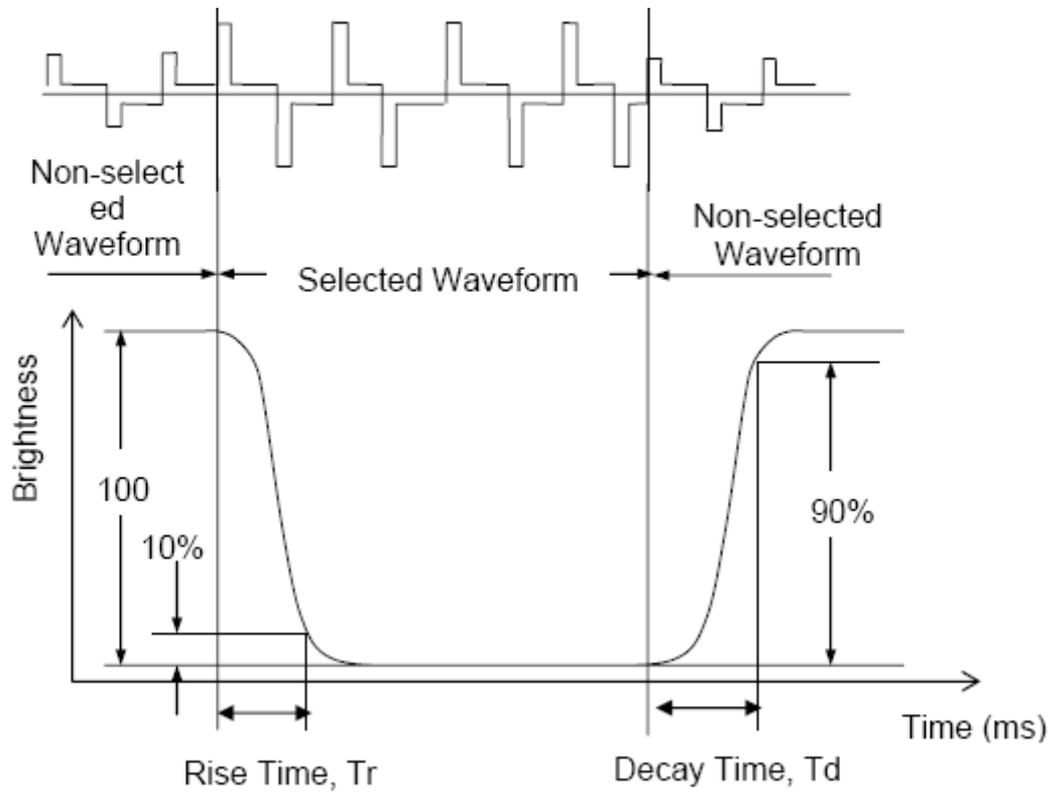
.Note3.Definition of Viewing Angle θ and φ：

12 O'clock Direction
$\varphi = 180°$

θ

$\varphi = 270°$
9 O'clock Direction

$\varphi = 90°$
3 O'clock Direction

φ

$\varphi = 0°$

6 O'clock Direction

Note4.Definition of Contrast ratio (CR):

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$
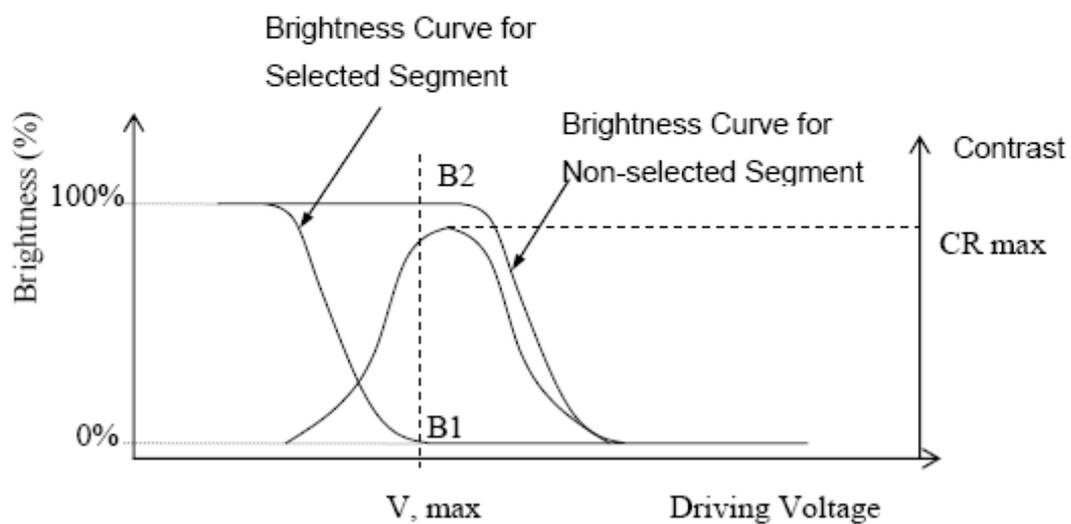
10. Reliability

10.1Mtbf

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal

10.2Test condition

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Non-Operating Test	80℃*240Hrs	。No Defect Of Operational Function In Room Temperature Are Allowable
2	Low Temperature Non-Operating Test	-30℃*240Hrs	
3	High Temperature/Humidity Non Operating Test	60℃*90%RH*240Hrs	
4	High Temperature Operating Test	70℃*240Hrs	。IDD of LCM in Pre-and Post-Test Should Follow Specification
5	Low Temperature Operating Test	-20℃*240Hrs	
6	Thermal Shock Test	-20℃(30Min) ↔70℃(30Min) *10CYCLES	

Notes:

1. Judgments should be made after exposure in room temperature for two hours.

2. The distill water is used for the high temperature/humidity test.

3. The sample above is individually for every reliability tests condition.

11.Inspection standards

1.AQL(Acceptable Quality Level

AQL of major and minor defect.

	MAJOR DEFECT	MINOR DEFECT
AQL	0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, the lux is 1000 ± 200.(Darkroom's lux: 100 ± 50),About an angle of incidence 30,a distance of 30 cm with an angle of 45 degree to check the products without uncovering the film!
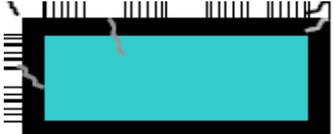
(As shown below)
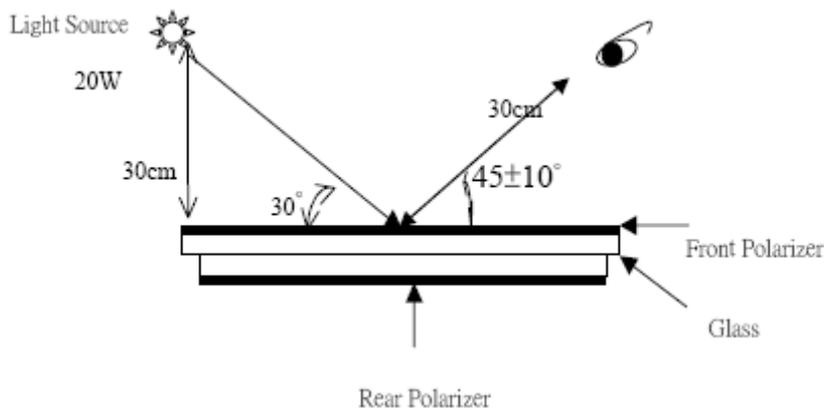
3.Inspection item and criteria
3.1 Visual inspection criterion in immobility

3.1.1Glass defect

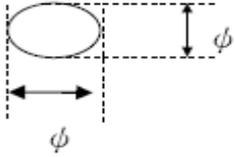| NO	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	
2	Cracks (Major defect)	1. Linear cracks panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage. 1) b≤1/3Pin width(non bonding area)	A: Length, b: Width

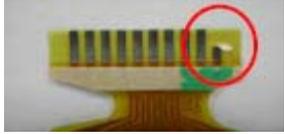|		2)bonding area≤0.5mm【Accept】【Accept】	
4	Pin-side ,conductive area damaged (minor defect)	(a c: disregards) b≤1/3of effective length for bonding electrode 【Accept】	a: length, b: Width, c: Thickness
5	Pin-side,non-conductive area damaged (minor defect)	1)Damage area don't touch the ITO (Inclueling contraposition mark, except scribing mark) 【Accept】 2)C<T b≦BM1/3of width 【Accept】 3)c=T b not touch the seal glue 【Accept】 4)a disregards	a: Length, b: Width c: Thickness
6	Non-pin-side damage (minor defect)	c<T 1)b exceeds 1/3Bm 【Reject】 c=T b not touch the seal glue 【Reject】	c: Thickness b: width of BM 内緣 damage

3.1.2LCD appearance defect(View area)

NO	Defect item	Criteria		Remark
		Specification	Allowable	note1:L: Length, W: Width
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note2: disregard if out of AA
		0.03mm<W≦0.05mm; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm;L>3.0mm	0	
2	Polarizer bubble、concave and convex	Φ≦0.2mm	disregard	note1: Φ=(L+W)/2,L:Length, W :Width
		0.2mm<Φ≦0.3mm	2	

	(minor defect)	0.3mm< Φ ≦0.5㎜	1	note2:disregard if out of AA
		0.5mm< Φ	0	
3	Black dots、dirty dots、impurities、eye winker (minor defect)	Φ ≦0.15mm	disregard	note2:disregard if out of AA
		0.15mm< Φ ≦0.25㎜	2	
		0.25mm< Φ ≦0.3㎜	1	
		0.3mm< Φ	0	
4	Polarizer prick (minor defect)	Φ ≦0.1mm	disregard	note1: Φ=(L+W)/2, L=Length, W=Width
		0.1mm< Φ ≦0.25㎜	3	note2:the distance between two dots>5mm
		Φ >0.25㎜	0	

3.1.3FPC

NO	Defect item	Criteria		Remark
1	Copper screen peel (minor defect)	Copper screen peel 【Reject】		
2	No release tape or peel	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	Note1: Cannot have stride ITO impurities
		Φ ≦0.25mm	2	
		Φ >0.25	0	

3.1.4Black tape &Mara tape

NO	Defect item	Criteria	Remark
1	FPC or H/S black tape (minor defect)	1. shift spec: 1) glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1)exceed of FPC edge or H-S edge【Reject】 2) IC bare 【Reject】	
2	No black tape (major defect)	No black tape 【Reject】	
3	Tape position mistake	Not by engineering drawing	
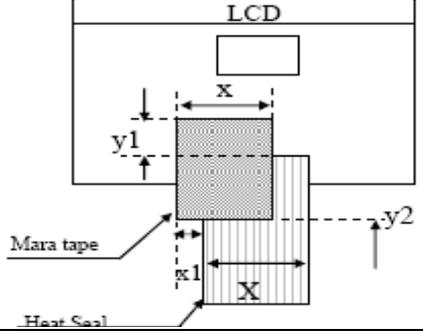
		(minor defect)	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film 【Reject】	

3.1.5Silicon and Taffy glue

NO	Defect item	Criteria	Remark
1	Quantity of silicon (major defect)	Uncover the ITO and circuit area 【Reject】	note: compared by engineering
2	Taffy glue (major defect)	1.Uncover the reveal copper area【Reject】 2.Cover layer 0.3mm(Min)~3.0mm(Max) 【Reject】	note: if customer has special requirement, refer to the technical document 3.0mm(Max)
3	Depth of glue covering (major defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement
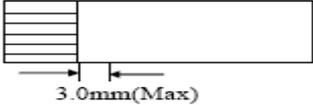
3.2Electrical criteria

NO	Defect item	Criteria	Remark
1	No display (major defect)	No display 【Reject】	
2	Missing line (major defect)	Missing line 【Reject】	
3	Seg-com light and dark (major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (major defect)	Flicker of Pattern 【Reject】	
6	Mura (major defect)	ND filter 2%test	
7	Over current (major defect)	Over current 【Reject】	
8	Voltage out of specification (major defect)	Voltage out of specification 【Reject】	

9	Pattern blur, error code (major defect)	Pattern blur, error code 【Reject】		
10	Dark light, Flicker (major defect)	Dark light, Flicker 【Reject】		
11	Black/white dots 、 Dirty dots、eye winker (major defect)	Specification	Allowable	Note1:disregard if out of AA
		Φ≦0.15mm	disregard	
		0.15mm<Φ≦0.25mm	2	
		0.25mm<Φ≦0.3mm	1	
		0.3mm<Φ	0	
12	Fiber、glass crutch、Polarizer scratch/folded (major defect)	W≦0.03mm	disregard	Note1:L: Length, W: Width Note2: disregard if out of AA
		0.03mm<W≦0.0.05mm L≦3.0mm	2	
		0.05mm<W≦0.1mm L≦3.0mm	1	
		W>0.1mm;L>3.0mm	0	

12.Precautions for using LCD modules.

12.1 Safety

(1)Do mot swallow any liquid crystal ,even if there is no proof that liquid crystal is poisonous.

(2)If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.

(3)If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

12.2Srorang Conditions

(4)Store the panel or module in a dark place where the temperature is 23±5℃and the humidity is below 45±20%RH.

(5)Store in anti-static electricity container.

(6)Store in clean environment, free from dust, active gas, and solvent.

(7)Do not place the module near organics solvents or corrosive gases.

(8))Do not crush, shake, or jolt the module.

12.3Handling Precautions

(9) Avoid static electricity, which can damage the CMOS LSI.

(10) The polarizing plate of the display is very fragile, please handle if very carefully.

(11) Do not give external shock.

(12) DO mot apply excessive force on the surface.

(13) Bo not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

(14) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

(15) Do not operate it above the absolute maximum rating.

(16) Do not remove the panel or frame from the module.

12.4 Warranty

The period is within twelve months since the date of shipping out under normal using and storage conditions.

13. Factory

FACTORY NAME:

FACTORY ADDRESS:

FACTORY PHONE:

14. Revision history

Version	Revise record	Date
v0.0	Original version	2020-12-16