



文件名称	BLU Purchase Specification 模组规格书	页次	1/17
产品名称	HBM185FH10A	版次	1.1

规格书 Specification Sheet

客户：

(Customer Name)

品名：

(Material Name)

料号：

(Material Number)

客户料号

(Customer Material Number)

客户承认 Customer			
<i>Approved by</i> 承认	<i>Checked by</i> 审核	<i>Approved by</i> 承认	
		<i>Checked by</i> 审核	
		<i>Designed by</i> 编写	

文件名称	BLU Purchase Specification 模组规格书	页次	3/17
产品名称	HBM185FH10A	版次	1.1

Contents

<i>No</i>	<i>ITEM</i>	<i>Page</i>
	<i>REVISIONS HISTORY</i>	<i>2</i>
	<i>CONTENTS</i>	<i>3</i>
<i>1</i>	<i>GENERAL DESCRIPTION</i>	<i>4</i>
	<i>1.1 Introduction</i>	
	<i>1.2 Features</i>	
	<i>1.3 Applications</i>	
	<i>1.4 General Specification</i>	
<i>2</i>	<i>ABSOLUTE MAXIMUM RATINGS</i>	<i>6</i>
<i>3</i>	<i>ELECTRICAL SPECIFICATIONS</i>	<i>7</i>
	<i>3.1 TFT LCD Open Cell</i>	
<i>4</i>	<i>INTERFACE CONNECTION</i>	<i>8</i>
	<i>4.1 Open Cell Input Signal & Power</i>	
	<i>4.2 LVDS Rx Interface Timing Parameter</i>	
<i>5</i>	<i>SIGNAL TIMING SPECIFICATIONS</i>	<i>10</i>
	<i>5.1 Timing Parameters (DE only mode)</i>	
	<i>5.2 Signal Timing Waveform</i>	
	<i>5.3 Power Sequence</i>	
<i>6</i>	<i>OPTICAL SPECIFICATIONS</i>	<i>14</i>
<i>7</i>	<i>2D Drawing</i>	<i>15</i>

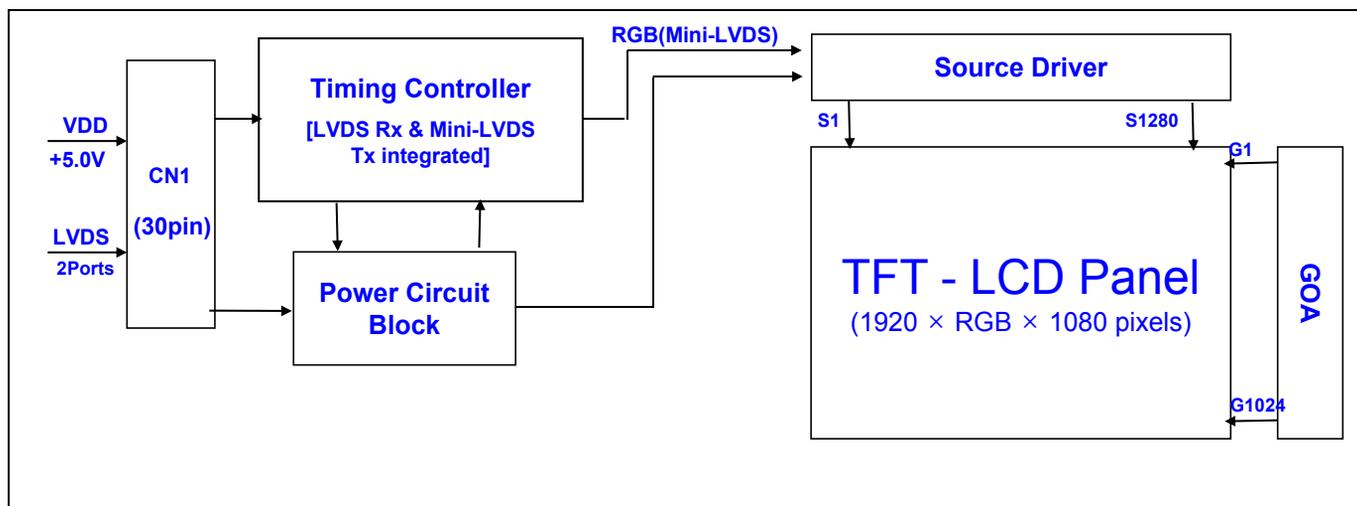
SPEC. NUMBER	SPEC. TITLE HBM185FH10A Product Specification Rev.P0	PAGE 3 OF 15
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文件名称	BLU Purchase Specification 模组规格书	页次	4/17
产品名称	HBM185FH10A	版次	1.1

1.0 GENERAL DESCRIPTION

1.1 Introduction

QV185FHB-N81 is a color active matrix TFT LCD MDL using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This Open Cell has a 18.5 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- Wide viewing angle
- DE (Data Enable) only mode
- HADS technology is applied for high display quality
- RoHS compliant

SPEC. NUMBER	SPEC. TITLE	PAGE
DAS-RD-2019028-O	HBM185FH10A Product Specification Rev.P0	4 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	5/17
产品名称	HBM185FH10A	版次	1.1

1.3 Application

- Commercial Digital Display
- Display Terminals for Control System
- Landscape and Portrait Display

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remarks
Active area	408.96 (H) × 230.04 (V)	mm	
Number of pixels	1920(H) × 1080(V)	pixels	
Pixel pitch	213(H) × 213(V)	um	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M	colors	Real 8bits
Display mode	Normally Black		
Dimensional outline	430.4(H) × 254.6(V) × 0.8(D)	mm	Detail refer to drawing
Weight	TBD	g	
Sealing Area	6.69/5/6.62/6.62	mm	U/D/L/R
Surface Treatment	Haze 25%		

SPEC. NUMBER

SPEC. TITLE

HBM185FH10A Product Specification Rev.P0

PAGE

5 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	6/17
产品名称	HBM185FH10A	版次	1.1

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	6.0	V	Ta = 25 °C
Logic Supply Voltage	VIN	VSS-0.3	VDD+0.3	V	
Operating Temperature	T _{OP}	0	+50	°C	Note 1
Storage Temperature	T _{SUR}	-20	+60	°C	
	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

文件名称	BLU Purchase Specification 模组规格书	页次	7/17
产品名称	HBM185FH10A	版次	1.1

3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25 ± 2 °C]

Parameter	Symbol	Values			Unit	Remark	
		Min	Typ	Max			
Power Supply Input Voltage	VDD	4.5	5.0	5.5	Vdc		
Power Supply Ripple Voltage	VRP	-	-	200	mV		
Power Supply Current	IDD	-	400	1000	mA	Note 1	
Power Consumption	PDD	-	2	5	Watt		
Rush current	IRUSH	-		3.0	A	Note 2	
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100	-	+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300	-	-100	mV	
	Input Differential Voltage	VID	200	-	600	mV	
	Differential input common mode voltage	VCM	1.0	1.2	1.5	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=5.0V,

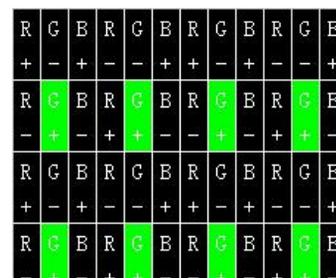
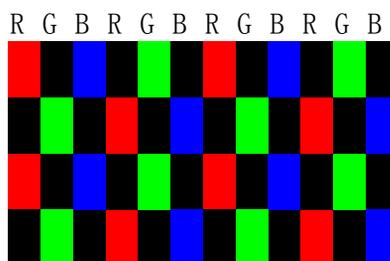
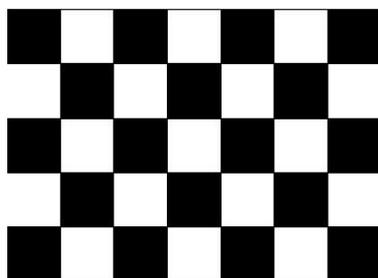
Frame rate $f_v=60\text{Hz}$ and Clock frequency = 74.25MHz.

Test Pattern of power supply current

a) Typ : Mosaic 7X5 (L0/L255)

b) Max : Skip 1 dot Pattern

c) Flicker Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

SPEC. NUMBER

SPEC. TITLE

HBM185FH10A Product Specification Rev.P0

PAGE

7 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	8/17
产品名称	HBM185FH10A	版次	1.1

4.0 INTERFACE CONNECTION

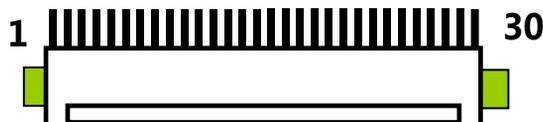
4.1 Open Cell Input Signal & Power (CN101)

- LVDS Connector : IS100-L300-C23(UJU), MSBKT2407P30HC(STM) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	RX00-	Negative Transmission data of Pixel 0 (ODD)	16	RXE1+	Positive Transmission data of Pixel 1 (EVEN)
2	RX00+	Positive Transmission data of Pixel 0 (ODD)	17	GNG	Power Ground
3	RX01-	Negative Transmission data of Pixel 1 (ODD)	18	RXE2-	Negative Transmission data of Pixel 2 (EVEN)
4	RX01+	Positive Transmission data of Pixel 1 (ODD)	19	RXE2+	Positive Transmission data of Pixel 2 (EVEN)
5	RX02-	Negative Transmission data of Pixel 2 (ODD)	20	RXEC-	Negative Transmission Clock (EVEN)
6	RX02+	Positive Transmission data of Pixel 2 (ODD)	21	RXEC+	Positive Transmission Clock (EVEN)
7	GND	Power Ground	22	RXE3-	Negative Transmission data of Pixel 3 (EVEN)
8	RXOC-	Negative Transmission Clock (ODD)	23	RXE3+	Positive Transmission data of Pixel 3 (EVEN)
9	RXOC+	Positive Transmission Clock (ODD)	24	GND	Power Ground
10	RX03-	Negative Transmission data of Pixel 3 (ODD)	25	NC	No. Connection
11	RX03+	Positive Transmission data of Pixel 3 (ODD)	26	NC	No. Connection
12	RXE0-	Negative Transmission data of Pixel 0 (EVEN)	27	NC	No. Connection
13	RXE0+	Positive Transmission data of Pixel 0 (EVEN)	28	VDD	Power Supply: +5V
14	GND	Power Ground	29	VDD	
15	RXE1-	Negative Transmission data of Pixel 1 (EVEN)	30	VDD	

Note : Pin 24 should be connected with GND.



SPEC. NUMBER

SPEC. TITLE

HBM185FH10A Product Specification Rev.P0

PAGE

8 OF 15

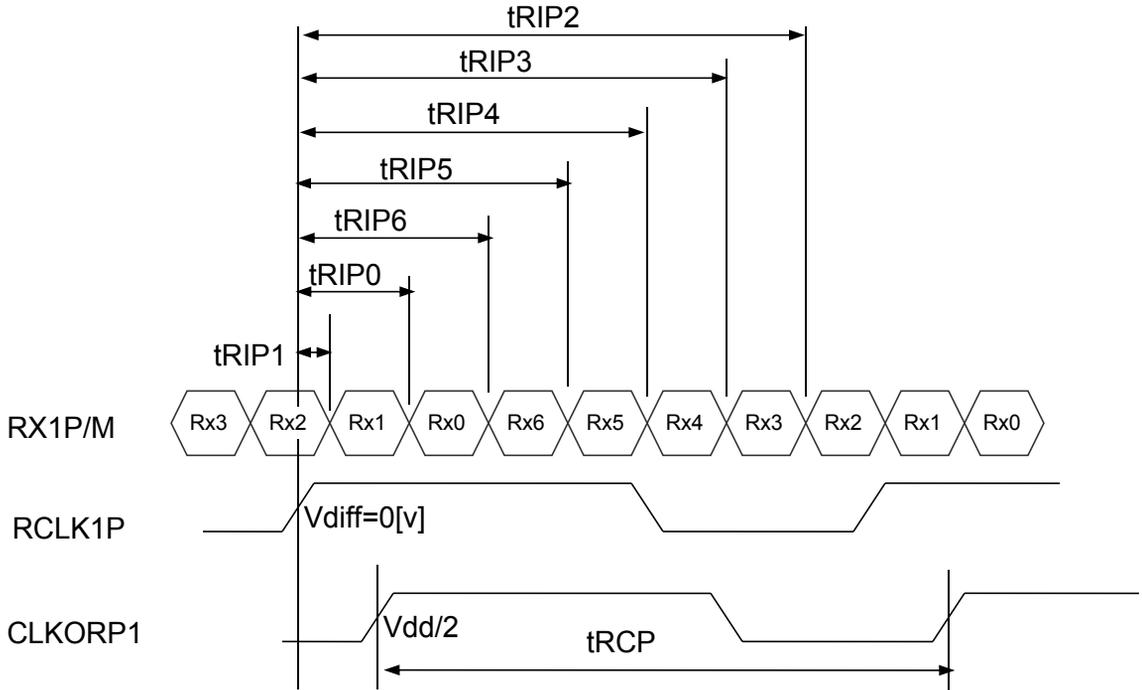
文件名称	BLU Purchase Specification 模组规格书	页次	9/17
产品名称	HBM185FH10A	版次	1.1

4.2 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 6. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	14.8	18.5	22.2	nsec	
Receiver Data Input Margin	tRMG	-0.35	-	0.35	nsec	fCLKIN=110MHz
		-0.40	-	0.40	nsec	fCLKIN=95MHz
		-0.45	-	0.45	nsec	fCLKIN=85MHz
		-0.60	-	0.60	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	- tRMG	0.0	tRMG	Clock	
Input Data 1	tRIP0	T/7- tRMG	T/7	T/7+ tRMG	Clock	
Input Data 2	tRIP6	2 T/7- tRMG	2T/7	2T/7+ tRMG	Clock	
Input Data 3	tRIP5	3T/7- tRMG	3T/7	3T/7+ tRMG	Clock	
Input Data 4	tRIP4	4T/7- tRMG	4T/7	4T/7+ tRMG	Clock	
Input Data 5	tRIP3	5T/7- tRMG	5T/7	5T/7+ tRMG	Clock	
Input Data 6	tRIP2	6T/7- tRMG	6T/7	6T/7+ tRMG	Clock	



* Vdiff = (RXz+)-(RXz-),.... ,(RXCLK+)-(RXCLK-)

文件名称	BLU Purchase Specification 模组规格书	页次	10/17
产品名称	HBM185FH10A	版次	1.1

5.0 SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Table 8. Timing Table >

Item		Symbols	Min	Typ	Max	Unit	
Clock	Frequency	1/Tc	60	74.25	78	MHz	
	High Time	Tch	-	4/7Tc	-		
	Low Time	Tcl	-	3/7Tc	-		
Frame Period		Tv	1100	1125	1149	lines	
			48.5	60	63	Hz	
Horizontal Active Display Term		Valid	t _{HV}	-	960	-	t _{CLK}
		Total	t _{HP}	1060	1100	1200	t _{CLK}
Vertical Active Display Term		Valid	t _{VV}	-	1080	-	t _{HP}
		Total	t _{VP}	1100	1125	1149	t _{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

< Table 9. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T _{LVSK}	LVDS channel to channel skew	F=100MHz V _{IC} =1.2V V _{ID} =±400mV	-380	-	+380	ps
F _{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F _{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T _{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

SPEC. NUMBER

SPEC. TITLE

HBM185FH10A Product Specification Rev.P0

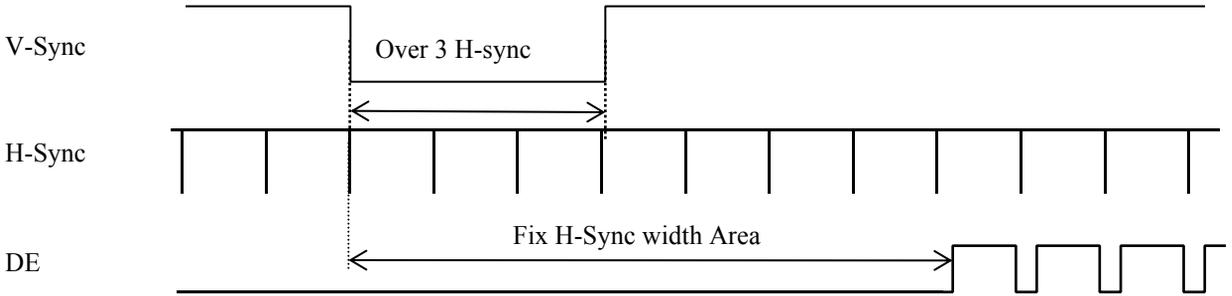
PAGE

10 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	11/17
产品名称	HBM185FH10A	版次	1.1

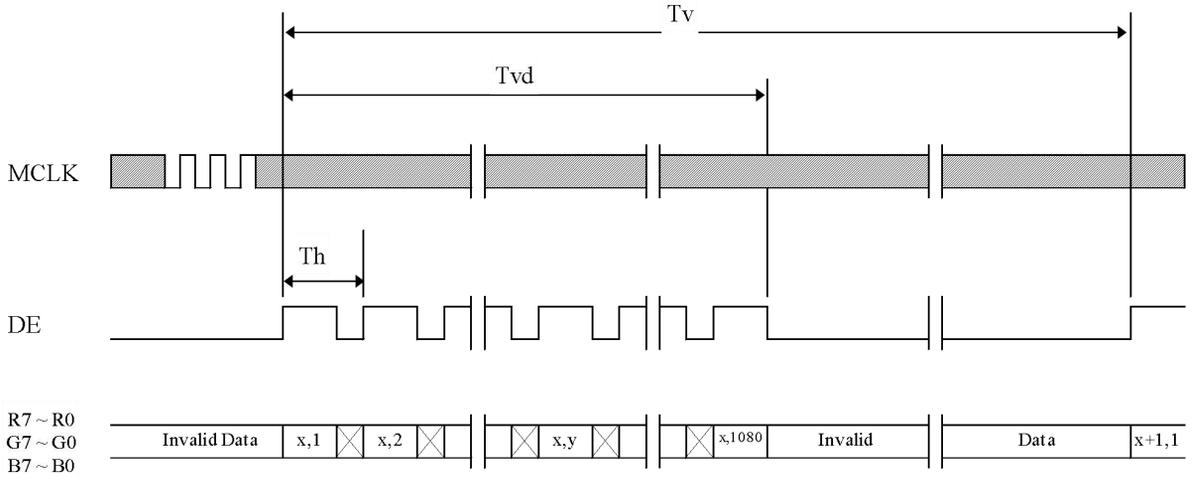
5.2 Signal Timing Waveform

5.2.1 Sync Timing Waveforms



- 1) Need over 3 H-sync during V-Sync Low
- 2) Fix H-Sync width from V-Sync falling edge to first rising edge

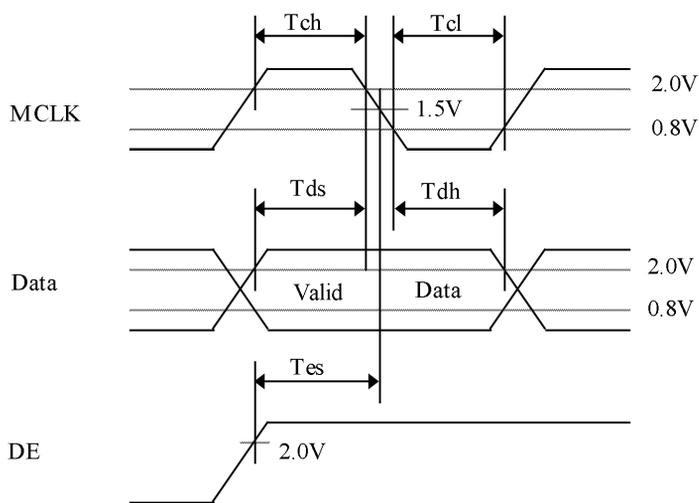
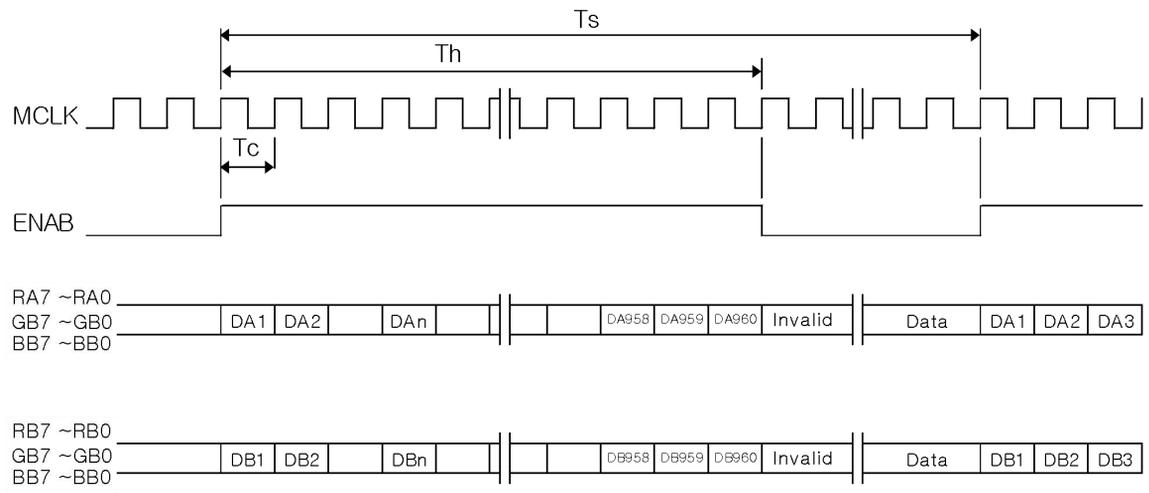
5.2.2 Vertical Timing Waveforms



SPEC. NUMBER	SPEC. TITLE	PAGE
DAS-RD-2019028-O	HBM185FH10A Product Specification Rev.P0	11 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	12/17
产品名称	HBM185FH10A	版次	1.1

5.2.3 Horizontal Timing Waveforms

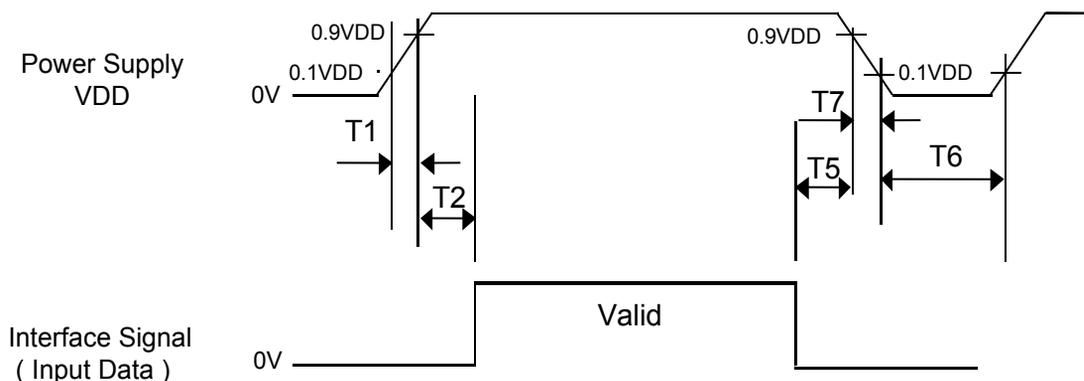


SPEC. NUMBER	SPEC. TITLE	PAGE
DAS-RD-2019028-O	HBM185FH10A Product Specification Rev.P0	12 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	13/17
产品名称	HBM185FH10A	版次	1.1

5.3 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 11. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

- Notes:
1. Back Light must be turn on after power for logic and interface signal are valid.
 2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
 3. When $VDD < 0.9VDD$ (Typ.), Power off.
 4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

SPEC. NUMBER	SPEC. TITLE	PAGE
DAS-RD-2019028-O	HBM185FH10A Product Specification Rev.P0	13 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	14/17
产品名称	HBM185FH10A	版次	1.1

6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance 1 lux and temperature=25 ±2°C) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{\Phi=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\Phi=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\Phi=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\Phi=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V at 25°C. Optimum viewing angle direction is 6 o'clock.

< Table 12. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 °C]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark	
Viewing Angle	Horizontal	θ_3	CR > 10	80	89	-	Deg.	Note 1	
		θ_9		80	89	-	Deg.		
	Vertical	θ_{12}		80	89	-	Deg.		
		θ_6		80	89	-	Deg.		
Brightness		Lv	$\theta = 0$ (Center) Normal Viewing Angle	350	400	-	nit		
Contrast ratio		CR		700:1	1000:1	-		Note 2	
White luminance uniformity		ΔY		75	80	-	%	Note 3	
Reproduction of color	White	W_x		TYP. - 0.03	TYP. + 0.03	TBD			Note 4
		W_y				TBD			
	Red	R_x				TBD			
		R_y				TBD			
	Green	G_x	TBD						
		G_y	TBD						
	Blue	B_x	TBD						
		B_y	TBD						
Color Gamut			68	72	-	%			
Cell Transmittance			TBD	TBD					
Response Time	G to G	T_g	-	14	20	ms	Note 5		

SPEC. NUMBER

SPEC. TITLE

HBM185FH10A Product Specification Rev.P0

PAGE

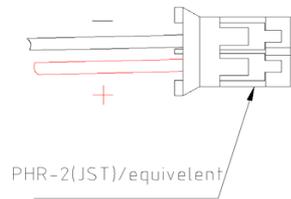
14 OF 15

文件名称	BLU Purchase Specification 模组规格书	页次	15/17
产品名称	21.5寸-2T模组规格书	版次	1.1

2. . BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Input Voltage Per Input Pin	VPIN	36	39.2	43	V	(1), Duty=100%, IPIN=(60mA)
灯条总电流 I	IPIN	---	320	360	mA	(1), (2) Duty=100%
LED Life Time	LLED	30000			Hrs	(3)
Power Consumption	PBL	12.6	---	---	W	(1) Duty=100%, IPIN=(60mA)

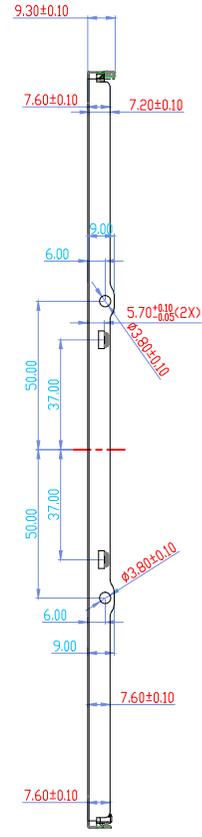
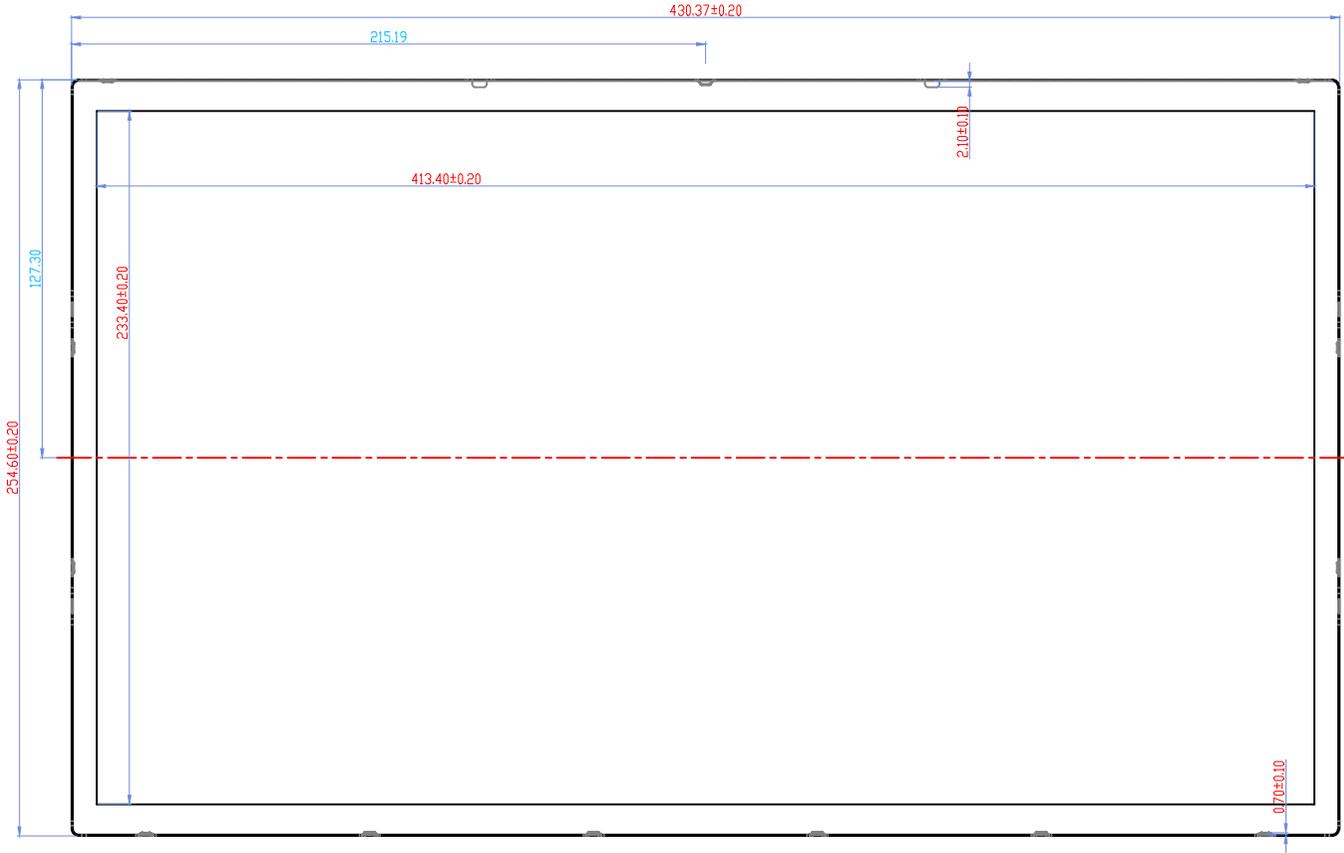
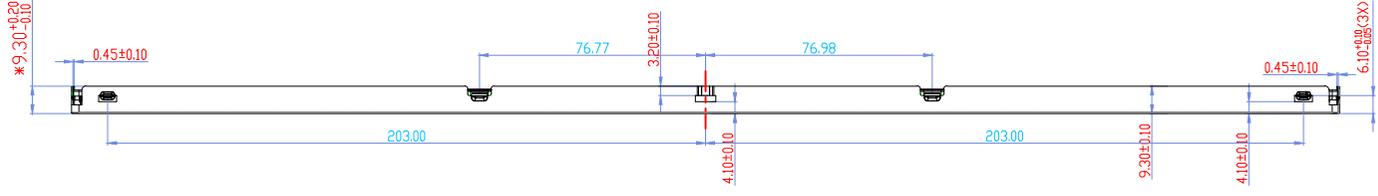
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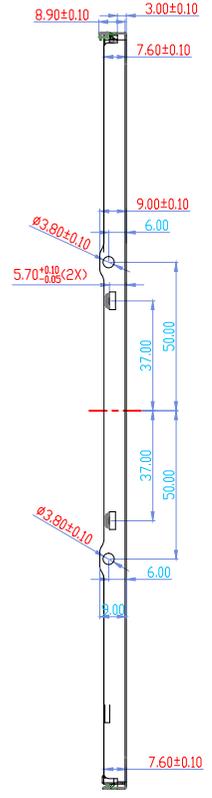
項目 Item	單位 unit	規格 Sption			备注 Remark		
		MIN	TYP	MAX			
1	模组亮度 BLU Brightness	Center point	cd/m ²	350	400	---	Center point (NOTE 1)
	均匀性 Uniformity	9点	%	72	75	---	(NOTE2)
2	模组色度 LCM CIE	x	---	-0.030	0.313	+0.030	Center point
		y	---	-0.030	0.329	+0.030	Center point

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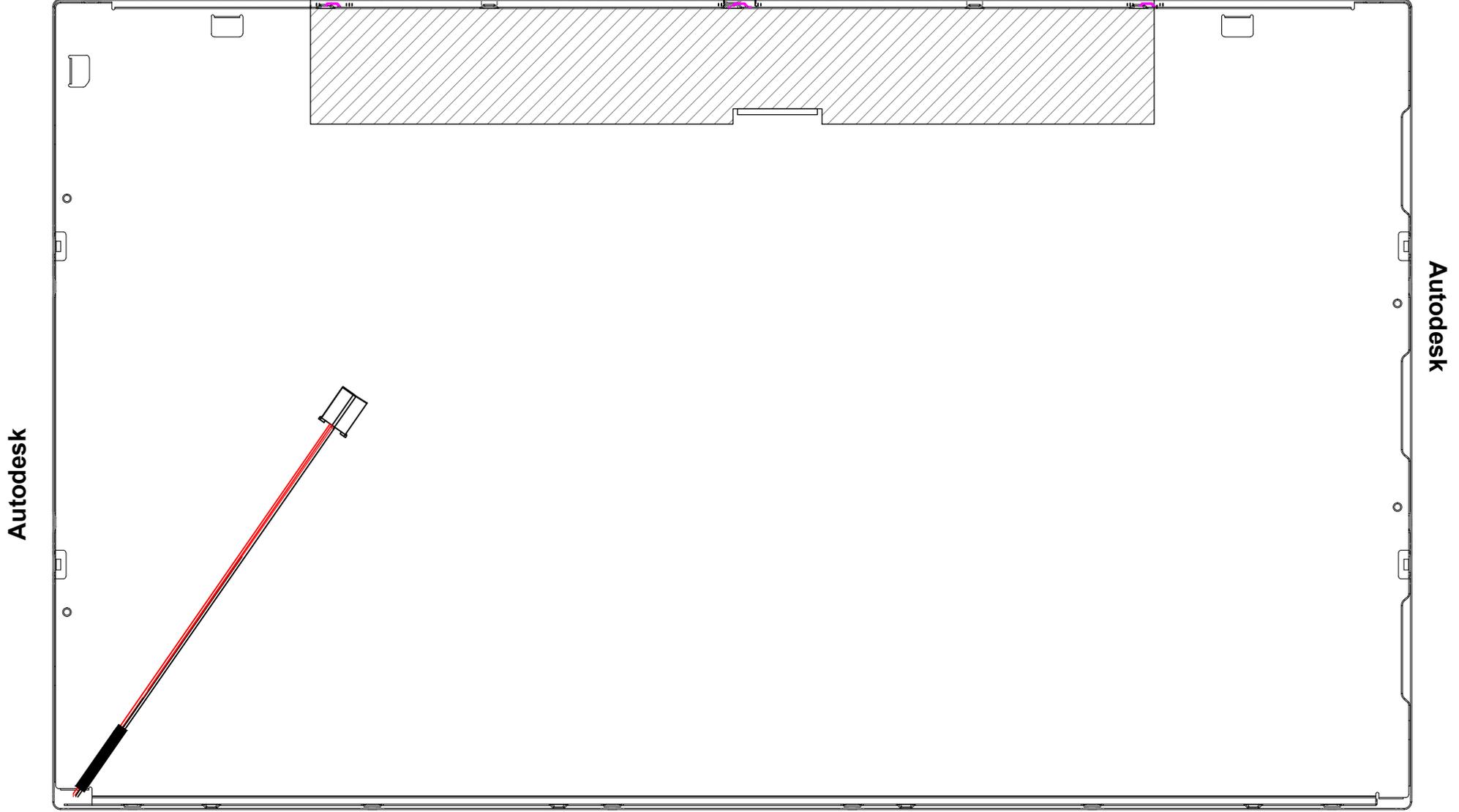
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