深圳市勋瑞光电科技有限公司
Xunrui photoelectric technology (shenzhen) CO,.LTD.

Product Specification

Customer: ______________________

Model Name: H055BFH30I5008

Date: 2024.10.30

Version: V0

■ **Preliminary Specification**

□ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

Contents

1. Record of Revision

Version	Revise Date	Content	Editor
V0	2024.10.30	First Release.	

2 General Specifications

Feature		Spec
Characteristics	LCD Size	5.5 inch
	Display Format	1080 (RGB) ×1920
	Interface	4 Lane MIPI
	Color Depth	16.7M
	Technology type	a-Si
	Display Spec.	-
	Display Mode	Normally BLACK
	Driver IC	R63350
	Surface Treatment	HC
	Viewing Direction	ALL
	Gray Viewing Direction	FREE
Mechanical	LCM+CTP (W x H x D) (mm)	77.80* 141.80 * 3.12
	LCM (W x H x D) (mm)	70.45* 127.85 * 1.47
	Active Area(mm)	68.04* 120.96
	With /Without TSP	With TSP
	Weight (g)	TBD
	LED Numbers	14 LEDs

Note 1: Viewing direction is following the data which measured by optics equipment.
Note 2: Requirements on Environmental Protection: RoHS
Note 3: LCM weight tolerance: +/- 5%

3 Input/Output Terminals

PIN No.	SYMBOL	Function
1	NC	No connection
2~3	VCC	Power supply
4	RST	Reset Signal pin ("Low" is enable)
5	NC	No connection
6	GND	Ground
7	D0N	DSI Data differential signal negative input pins. (Data lane 0-)
8	D0P	DSI Data differential signal positive input pins. (Data lane0+)
9	GND	Ground
10	D1N	DSI Data differential signal negative input pins. (Data lane 1-)
11	D1P	DSI Data differential signal positive input pins. (Data lane 1+)
12	GND	Ground
13	CLKN	DSI CLOCK differential signal negative input pins
14	CLKP	DSI CLOCK differential signal positive input pins
15	GND	Ground
16	D2N	DSI Data differential signal negative input pins. (Data lane 2-)
17	D2P	DSI Data differential signal positive input pins. (Data lane 2+)
18	GND	Ground
19	D3N	DSI Data differential signal input negative pins. (Data lane3-)
20	D3P	DSI Data differential signal positive input pins. (Data lane3+)
21	GND	Ground
22	NC	No connection
23~24	LEDK	Backlight LED Cathode
25~28	NC	No connection
29~30	LEDA	Backlight LED Anode.

4 Absolute Maximum Ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX	
Supply Voltage range	VDD	-0.3	-	4.6	V
Operating Temperature range	T_{OP}	-20	-	+70	℃
Storage Temperature range	T_{ST}	-30	-	+80	℃

5 Electrical Characteristics

5.1 DC Characteristics

Item	Symbol	Min.	Type.	Max.	Unit
Logic Supply Voltage	VCC	2.7	2.8	3.3	V
I/O Supply Voltage	IOVCC	1.65	1.8	3.3	V

注：复位电压需与 IOVCC 保持一致。

5.2 Driving Backlight

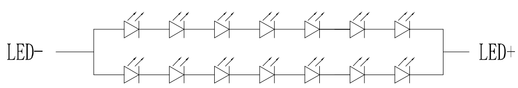
Item	Symbol	MIN	TYP	MAX	Unit	Remark
LED current	I_F	-	40	-	mA	Note 1 Note 2,3
LED Voltage	V_F	19	21	23	V	
Power Consumption	P	-	840	-	mW	
LED Life Time	T	20000	-	-	Hr	

Note 1 : There are 2 Groups LED

Note 2 : Ta = 25℃

Note 3 : Brightess to be decreased to 50% of the initial value

BACKLIGHT SCHEMATIC



CONSTANT CURRENT
(Vf=19V~23V) If=40mA

6 Interface Timing

6.1 MIPI Interface Timing Sequence

(a) MIPI interface DC characteristic

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	70	3
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	880	-	1350	
	I/O leakage current	ILEAK	µA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	450	-	-	

Notes:
1. VCMRX (DC) = (VP+VDN)/2
2. Excluding COG resistance (contact resistance and ITO wiring resistance). The values are tentative.
3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

(b) MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	2	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V DSI 2 lanes, 3 lanes, 4lane	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6

Notes:
4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
6. tSETUP/tHOLD Time are measured without HS-TX Jitter.

(C) MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVCC=DPHYVCC =1.65 ~ 3.30V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		IOVCC=DPHYVCC =1.65 ~ 3.30V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$		IOVCC=DPHYVCC =1.65 ~ 3.30V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11after HS burst	$T_{HS-EXIT}$	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVCC=DPHYVCC =1.65 ~ 3.30V	4*T_{LPTX}			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=DPHYVCC =1.65 ~ 3.30V	1*T_{LPTX}	-	2*T_{LPTX}	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=DPHYVCC =1.65 ~ 3.30V	5*T_{LPTX}			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	50	-	-	
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=DPHYVCC =1.65 ~ 3.30V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$		IOVCC=DPHYVCC =1.65 ~ 3.30V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=DPHYVCC =1.65 ~ 3.30V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=DPHYVCC =1.65 ~ 3.30V	-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=DPHYVCC =1.65 ~ 3.30V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=DPHYVCC =1.65 ~ 3.30V	-	1/(fosc/2)	-	

Notes:
1. If a > b then max (a, b) = a, otherwise max (a, b) = b
2. Where n = 1 for Forward-direction HS mode.
3. The R63350 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63350 can work without the remained process if tCLK-POST is more than 256 UI.
4. The R63350 uses DSI clock from the Host processor if Clock Lane is active and internal oscillator clock if Clock Lane is disabled

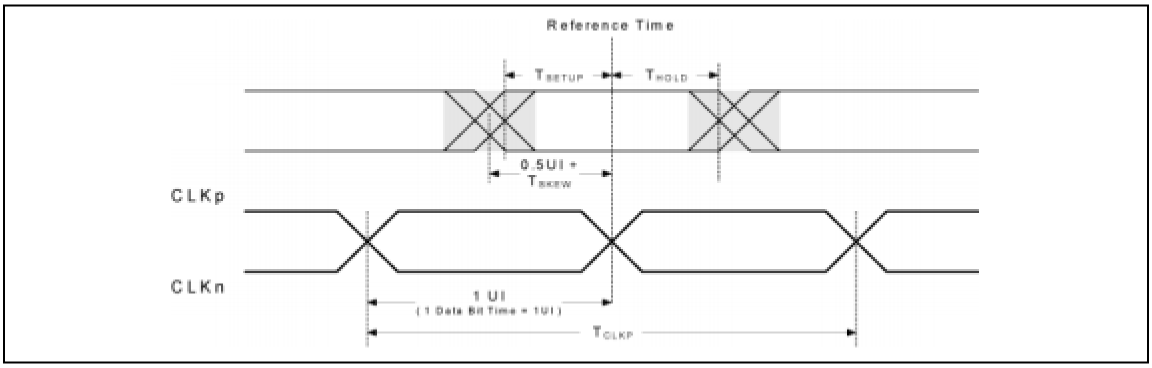


Figure Data to Clock Timing Definitions

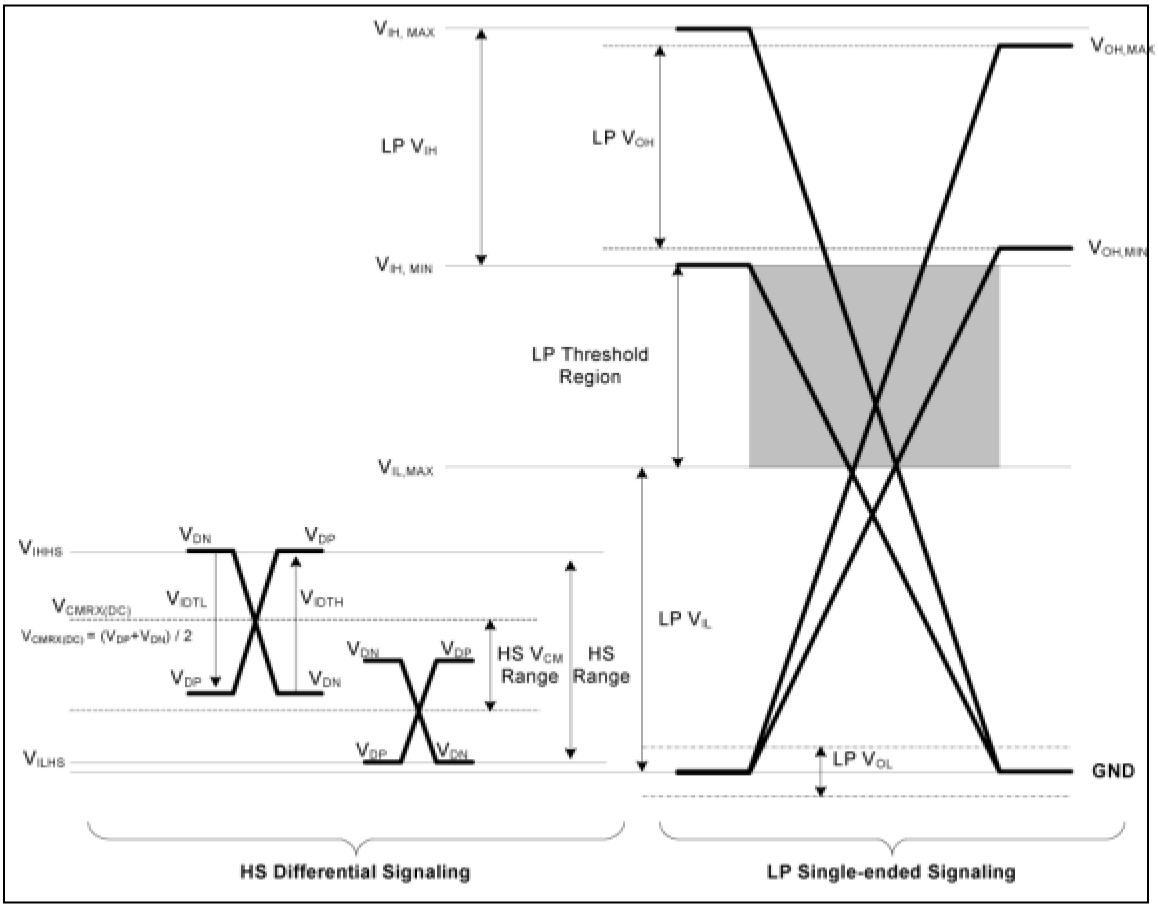


Figure DSI LP Mode

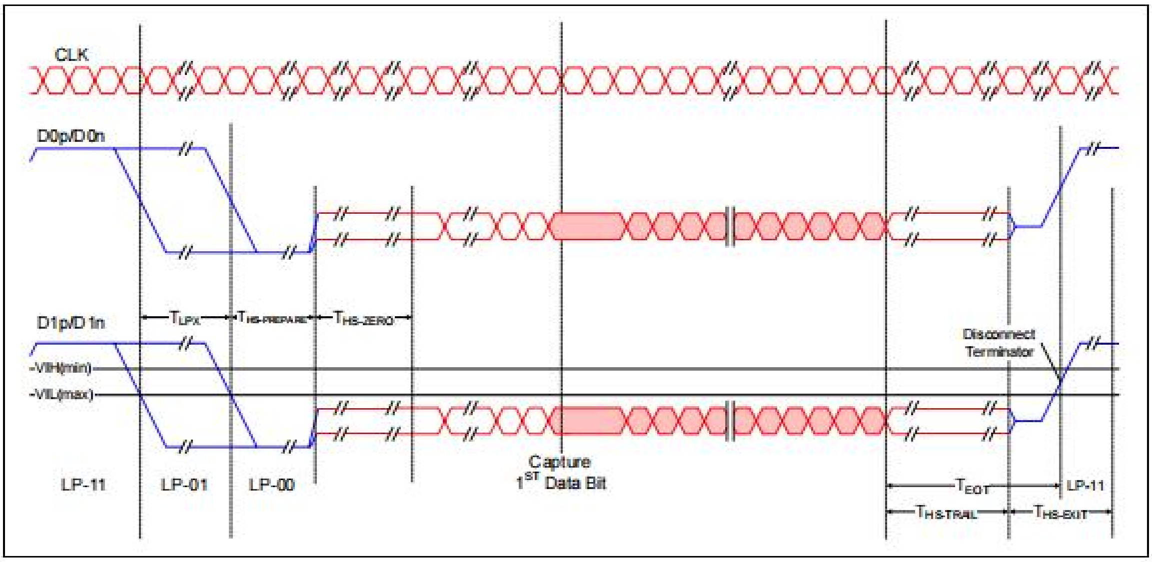


Figure HS Data Transmission in Bursts

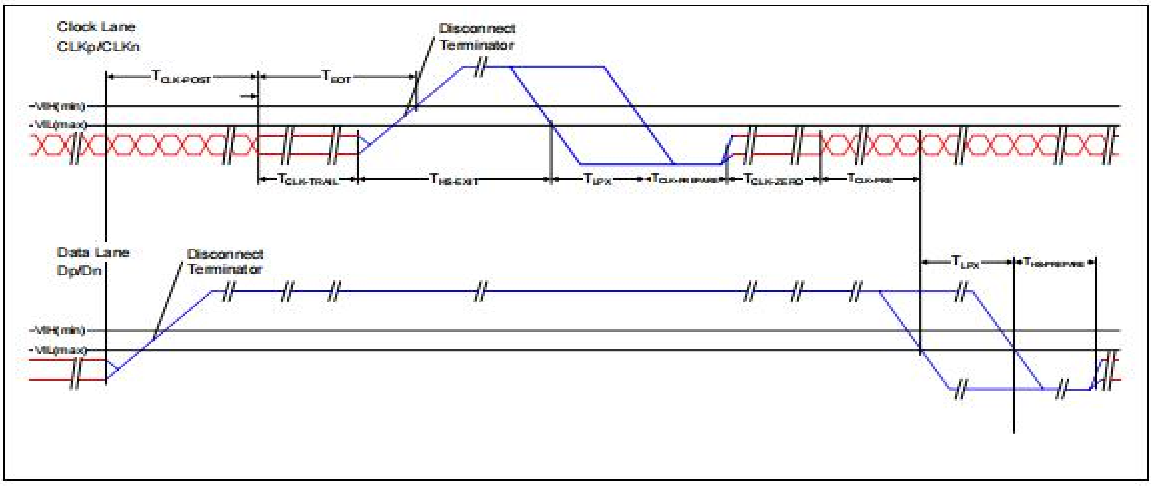


Figure Switching the Clock Lane between Clock Transmission and LP Mode

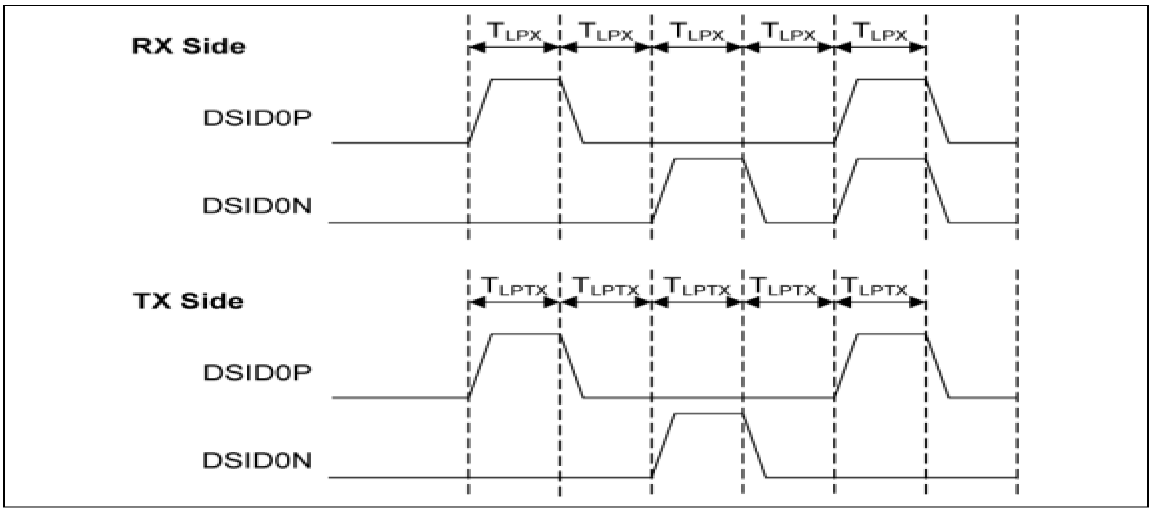
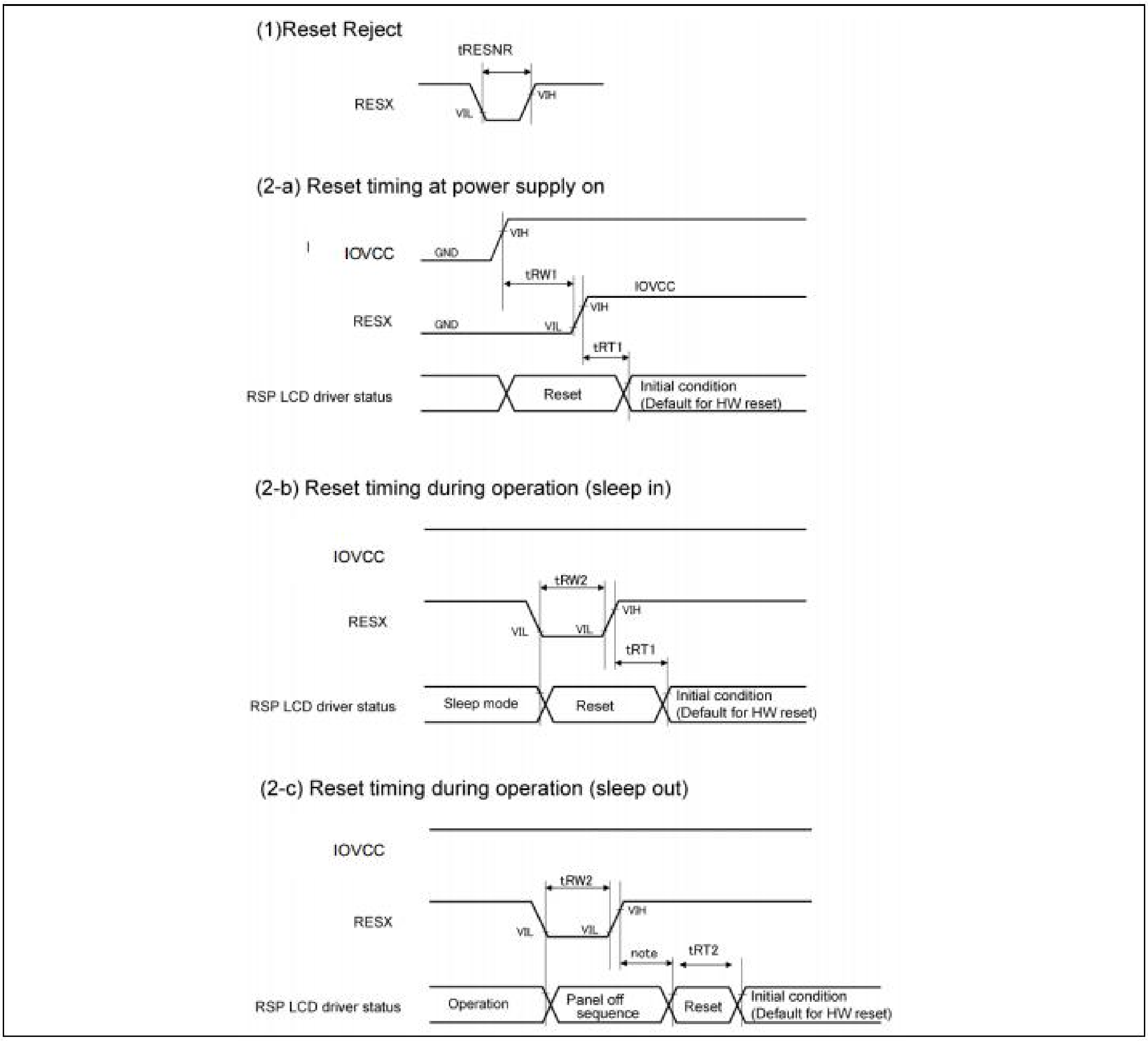


Figure DSI LP Mode

6.3 Reset Input Timing

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	–
Reset low-level width2	tRW2	us	Operation	1000	–
Reset time (Sleep IN)	tRT1	ms	–	–	3
Reset time (Sleep OUT)	tRT2	ms	–	–	3
Noise reject width	tRESNR	us	–	–	1



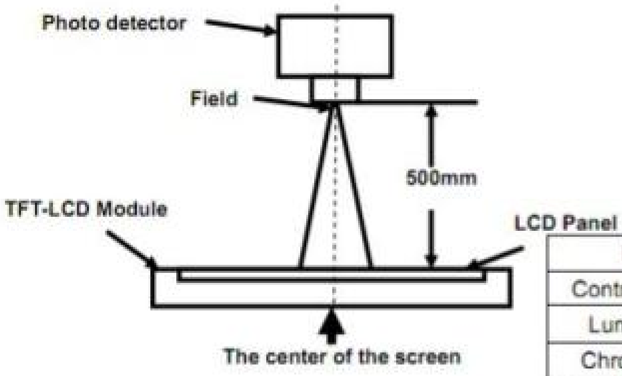
7 Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angles		θT	Center CR≥10	70	80	-	Degree.	Note2
		θB		70	80	-		
		θL		70	80	-		
		θR		70	80	-		
Contrast Ratio		CR	Θ =0	1000	1400		-	Note1, Note3
Response Time		$T_{R}+T_{F}$	25。C	-	30	35	ms	Note1, Note4
Chromaticity	White	X_W		0.247	0.287	0.327	-	Note1, Note5
		Y_W		0.272	0.312	0.352	-	
	Red	X_R		-	-	-	-	
		Y_R		-	-	-	-	
	Green	X_G		-	-	-	-	
		Y_G		-	-	-	-	
	Blue	X_B		-	-	-	-	
		Y_B		-	-	-	-	
Uniformity		U		75	80	-	%	Note1, Note6
NTSC				65	70		%	Note5
Luminance		L		450	500	-		Note1, Note7

Test Conditions:
1. IF= 20mA(one channel),the ambient temperature is 25°C.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical Properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	BM-7A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	SR-3A	2°

Note 2: Definition of viewing angle range and measurement system.
Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).

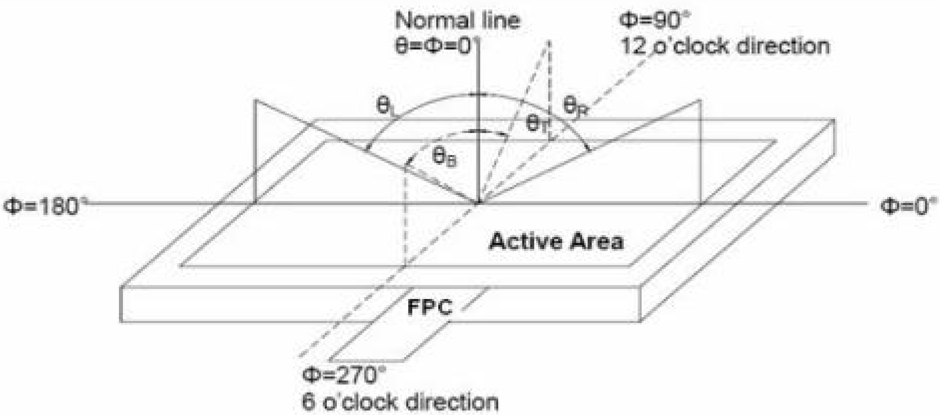


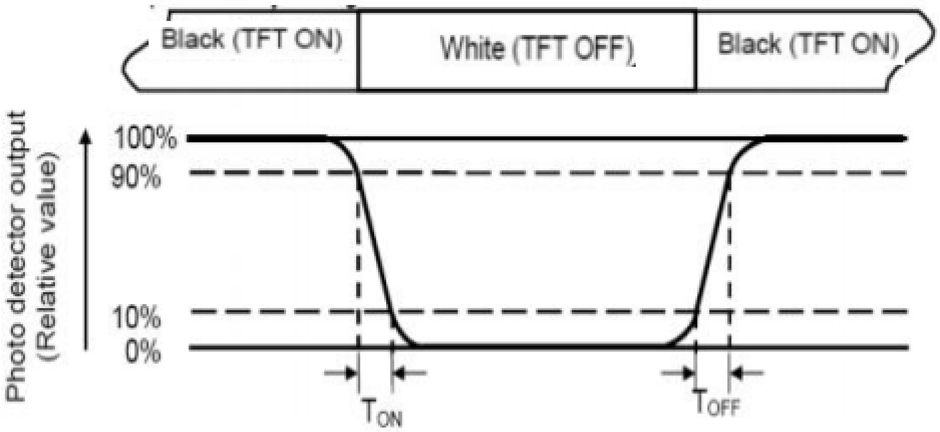
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval Between “White” state and “Black” state. Rise time (TON) is the time between Photo detector output intensity changed from 10% to 90%. And fall time (TOFF) is The time between photo detector output intensity changed from 90% to 10%



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the Center of each measuring area

Luminance Uniformity (U) = Lmin/ Lmax X100%

L-------Active area length W----- Active area width

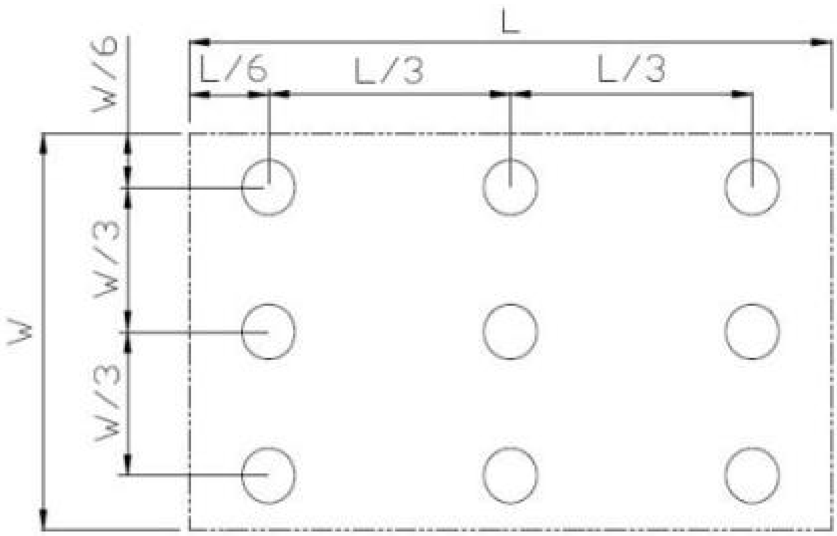


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 96hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 20 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. T_S is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.

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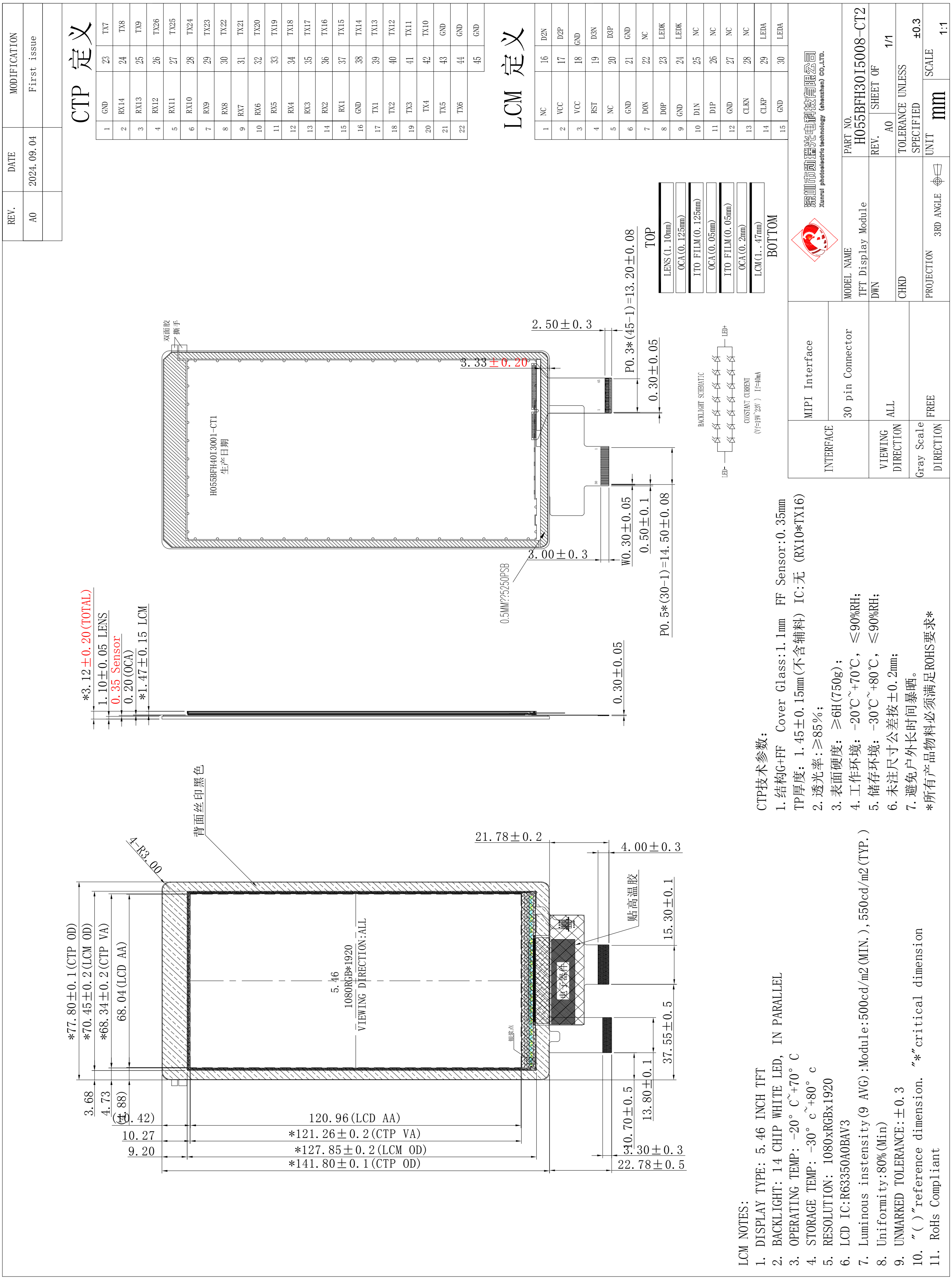
9 Mechanical Drawing



1 0.Packing

TBD

11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:
Water ； Ketene ； Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ~ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.